DEVELOPMENT OF CCD IMAGING SENSORS FOR SPACE APPLICATIONS Final Report—Phase I Contract JPL 953788

by Gault A. Antcliffe

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Prepared for Jet Propulsion Laboratory California Institute of Technology 4800 Oak Grove Drive Pacadena, California 91103

Texas Instruments Incorporated Central Research Laboratories Dallas, Texas 75222

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Final Report-Phase I

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ABSTRACI

This report describes the results of a predominantly experimental investigation made by Texas Instruments to develop a large-area charge-coupled device (CCD) imager for space photography applications. The levice developed under this phase of the contract, which will be referred to as Phase I and covered the period March 1974 to September 1975, was a 400 X 400 resolution element CCD. In the initial period of Phase I, a smaller 100 X 160 array was designed and fabricated to allow development of CCD technology which was then applied to the large array. The design used in the program was a three-phase buried-channel CCD, fabricated with an overlapping double-level metal electrode system. The CCDs were thinned and illuminated from the backside for maximum optical responsivity. Buried-channel operation provided charge-transfer efficiency greater than 0.9999. This resulted in excellent resolution capability at spatial frequencies up to the Nyquist limit at all elements of the 400 X 400 both near and far from the CCD output. Considerable development of CCD technology during this program resulted in 400 X 400 arrays with dark-current density below 1 nA/cm² at 24°C. Extensive optical evaluation of the arrays was performed at 24°C and -40°C and covered the frequency range 10 kHz to 1 MHz, depending on the particular parameter under investigation.

Details of the design and processing required to achieve 400 X 400 imagers are presented together with a discussion of the optical characterization techniques developed for this program. A discussion of several aspects of large CCD performance is given with detailed test reports which have been delivered to JPL during the course of the program. The areas covered include dark current, uniformity of optical response, square wave amplitude response, spectral responsivity, and dynamic range.



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10 December 1975

SECTION I INTRODUCTION

This report presents the results of a program funded by the Jet Propulsion Laboratory and performed by Texas Instruments over the period April 1974 to September 1975. The goal of the program was to develop a large-area charge-coupled device (CCD) imager for space photography applications.

Two arrays were designed and fabricated during the program. Initially, a CCD with 100 X 160 resolution elements was fabricated to allow the development of small resolution element (pixel) CCD technology. The experience gained with this array was then used to design and fabricate a much larger 400 X 400 element CCD. As a result of this contract, two types of CCD were made available to JPL. Operational CCDs, defined as not optically characterized in detail and fully characterized devices of both 100 X 160 and 400 X 400, were delivered. Three operational models of each of the 100 X 160 arrays and 400 X 400 arrays, three fully characterized 400 X 400 arrays and three operational 400 X 400 arrays were delivered for JPL evaluation during the program.

The device design chosen for this contract was the three-phase, double-level metal CCD, operating in the backside-illuminated mode. Backside illumination results in high and uniform spectral responsivity because incident illumination is focused on a uniform silicon backside surface rather than on a multilayered CCD electrode structure. Devices with high charge-transfer efficiency were achieved by operating in a buried-channel mode. The resolution element dimensions were 0.9×0.9 mil, using an active channel in the parallel section of 0.7 mil with 0.2 mil channel stops and three aluminum electrodes, each 0.3 mil in width. With this resolution element size, the active area of the 100×160 is 90×144 mils and for the 400×400 , it is 360×360 mil. The large array is fabricated on a silicon chip which is 0.5×0.5 inch.

This report is organized in the following way. In Section II the design of the 100 X 160 and 400 X 400 arrays is discussed together with details of the on-chip amplifiers and the fabrication of photomasks required for device processing. In Section III device fabrication is discussed together with details of failure modes for large-area CCDs and consideration of material perfection and oxide integrity. Section IV presents a brief discussion of buried-channel CCD operation to allow an indication of potential profiles in these devices from which many buried-channel operating parameters may be predicted. The details of the optical characterization facilities developed during this program and a discussion of the measurements made on the CCDs are presented in Section V. In Section VI, performance characteristics of the 160 X 160 and 400 X 400 arrays are discussed while results of the detailed test schedule applied to



100 X 160's and 400 X 400's are included as Appendixes A, B, C, D, E. These test reports were delivered to JPL progressively during the program.

The text of two technical presentations made during the course of the program and presented at the Symposium on the Scientific Application of CCDs in Pasadena and at the International Conference on CCDs in San Diego are included as Appendixes F and G.

A study relating to the extension of CCD technology to even larger arrays than the 400 X 400 and to extending blue response below 4000 Å is reported in Appendix H.



SECTION II DEVICE DESIGN

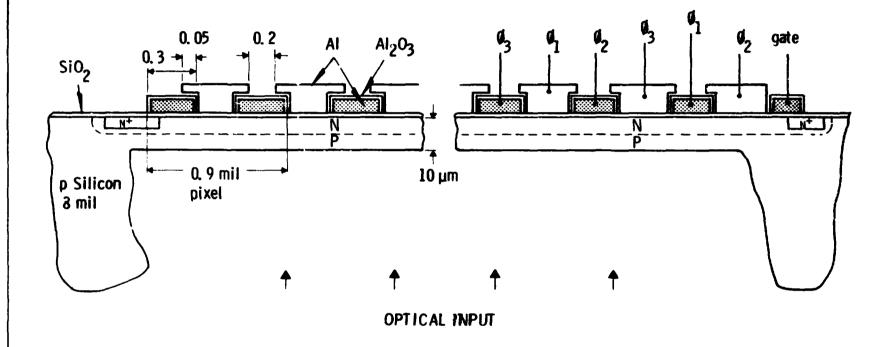
A. THREE-PHASE ARRAY DESIGN

Large-area charge-coupled device (CCD) imagers can be fabricated with any one of several existing technologies. 1,2,3 Since a completely sealed electrode structure is very desirable to optimize device electrical performance, many arrays use polysilicon electrodes that are sufficiently transparent to allow optical radiation to enter the active area of the CCD. Increased transmission through tin-indium oxide electrodes has also been observed. However electrode absorption and interference effects related to the device structure itself can result in degradation of optical performance particularly at short wavelengths. Illumination of the CCD from the backside eliminates this problem, but requires that the silicon chip be thinned over the active area of the CCD to a thickness less than one resolution element. For optimum performance, a thickness of 10 to $12 \,\mu\text{m}$ is used. The imagers fabricated under this contract were backside-illuminated, three-phase (3ϕ) CCDs fabricated using the double-level anodized aluminum technique. A completely sealed structure with high charge-transfer efficiency (CTE) and optimum optical responsivity is obtained. In this section, the 100 X 160 and 400 X 400 arrays developed under this contract will be described.

Both 160 X 100 and 400 X 400 imagers are n-channel, designed with a resolution element size (pixel) of 0.9 × 0.9 mil in the parallel imaging section. The maximum spatial frequency expected to be resolved by such a sampled imaging system is the Nyquist Frequency = 21.9 line pairs per millimeter. The CCD concept is shown schematically in Figure 2-1. An array of metallic transfer electrodes is formed over a SiO₂ gate oxide on a silicon substrate to allow charge to be transferred along the array. Charge packets (electrons) are held in depletion regions of each MOS capacitor as it is pulsed into depletion. Signal charge can be injected into the array by an n⁺ diode or by optical radiation falling on the backside of the array. After a period of time sufficient for the collection of optically generated signal charge (the integration time), the packets are transferred by appropriate clocking pulses to the depletion region of a reverse-biased (n⁺) output diode. The diode is connected to an on-chip amplifier. The silicon itself must be thinned over the CCD electrode region as shown in Figure 2-1 for high resolution since an excessive thickness of silicon will allow photogenerated electrons to diffuse in a lateral direction before collection in the potential wells of the CCD. Charge transport occurs at the junction of a shallow n layer and the p substrate to avoid surface-state transfer loss (buried-channel mode).

An important feature of 3ϕ design is that a given clocking phase occurs alternatively on a first-level and then a second-level electrode. First-level metal electrodes (shaded in Figure 2-1) are 0.3 mil in width and are formed by wet metal etching techniques in the first electrode processing step. These electrodes are subsequently coated with an anodically formed layer of Al_2O_3 . Second-level metal electrodes, each of width 0.4 mil, are then defined as shown. To ensure a sealed structure, an overlap of 0.05 mil is designed. This leaves a gap of 0.2 mil which must be opened by second-level etching. The implementation of these design dimensions is illustrated by a photomicrograph of the 100 X 160 chip in Figure 2-2. The array, which parallel section measures 90×144 mils, is centered on a 320×325 mil silicon chip with bond leads extending about 90 mils. This is done to allow a thinning window much larger than the light-sensitive array





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Figure 2-1. Schematic of Backside-Illuminated, 36, Double-Level-Aluminum CCD Imager



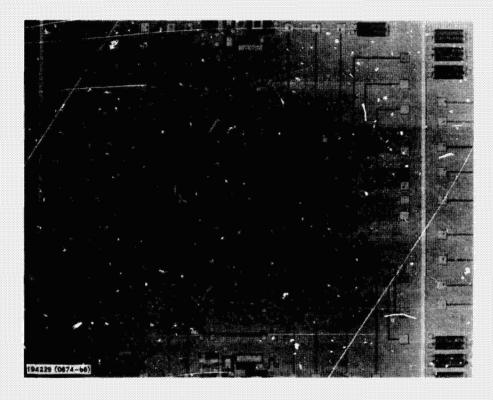


Figure 2-2. Photomicrograph of 100 X 160 imager

dimension. Two sets of test devices (MOSFETs and capacitors) are placed above and below the array. The organization of the array is serial-parallel-serial, which allows the input of electrical signals to the parallel section (Figure 2-3).

A double-level aluminum metalization separated by 2500 Å of Al_2O_3 forms the charge-transfer electrode structure. Three-phase clocking is used so that, in both parallel and serial sections of the array, a given phase occurs alternatively on first-level and second-level metal electrodes. The parallel section contains 160 columns and 301 metal transfer electrodes. This allows the last electrode at both the top and bottom of the array to be connected to the same clock phase (ϕ_3) . This feature allows the array to be operated either forward, using the lower serial register and BSHA output (Section II.C), or reverse, using CCA output by simply interchanging connections to ϕ_1 and ϕ_2 in the parallel section. Charge packets are transferred from ϕ_3 parallel into the potential well under ϕ_3 in either of the output serial registers. These output registers have 161 pixels so that the last serial electrode before the output gate is ϕ_2 . Signal charge is collected through the de-biased output gate on the fall of ϕ_2 (Section IV). The transfer gate region connecting serial and parallel sections is fabricated by a composite first- and second-level metalization. Charge is transferred through a 0.3 mil wide region 1.0 mil in length. It appears that this transfer results in no larger charge loss than is experienced in the normal CCD transfer sequence.

The 3ϕ design is implemented by using interconnection between first and second metal levels in desired areas which have been prevented from apodizing by areas of photoresist. These areas are defined on a via mask. Since all first-level metal is connected through the metalized



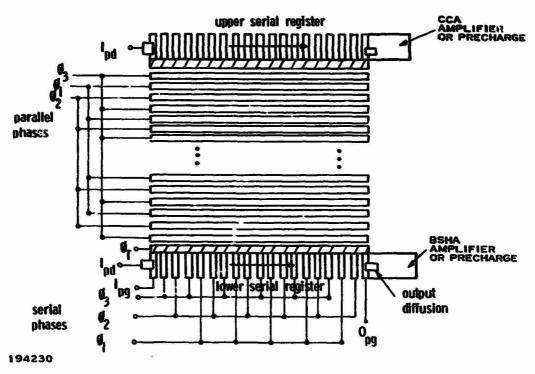


Figure 2-3. Serial-Parallel-Serial Organization of 100 X 160 and 400 X 400 CCD

scribe lines for the electrical continuity required in the anodization, desired regions are isolated by etching away at some of the unanodized via areas (bus cut mask). In simplified form these steps are shown in Figure 2-4 where the example is not intended to reflect any CCD configuration exactly but to illustrate busing three individual phases, ϕ_N to ϕ_{N+2} , from the same side of an electrode structure. The way in which a 3ϕ structure is implemented in the 160 X 100 and 400 X 400 imagers is shown in Figure 2-5 which is taken from a 500X Calcomp plot of the array itself. The parallel and serial regions are shown together with the composite transfer gate. The composite structure is dictated by the requirement that each channel in the parallel section transfers into the same serial phase. First and second levels are connected at the rectangular vias to form the composite. An earlier 3\phi array design (Conservative 100 X 160) had a single-level transfer gate but required charge from the parallel section to be injected into ϕ_3 and ϕ_2 in the serial for adjacent channels. The technique used to connect the serial electrodes to the three phase buslines is shown in Figure 2-5. Each electrode ϕ_n is connected at the via. This via is a region in which the first level is protected from anodizing by photoresist. This is subsequently removed and, when second-level metal is patterned, connection is made. Thus, all ϕ_n electrodes come out to single metalization leads. Connection to the outer busline is made on the first level while connection to the other two buslines are made by via and subsequent solation by removal of metal in the diagonal shaded areas. These "bus cuts" are necessary to isolate the metal electrodes since all metal after first level patterning must be connected so that the electrical contact necessary for anodization can be made. An input diode is provided at the input ends of each serial register to allow injection of electrical signals. Busing of the parallel electrodes is done in the same way as for the serial registers. Redundant busing,



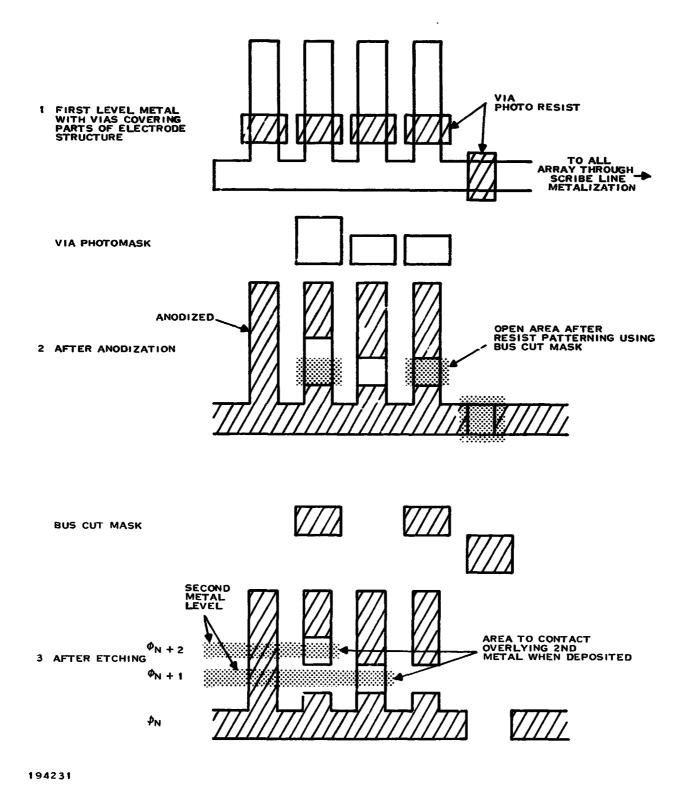


Figure 2-4. Example of Via and Bus Cut Steps in Processing



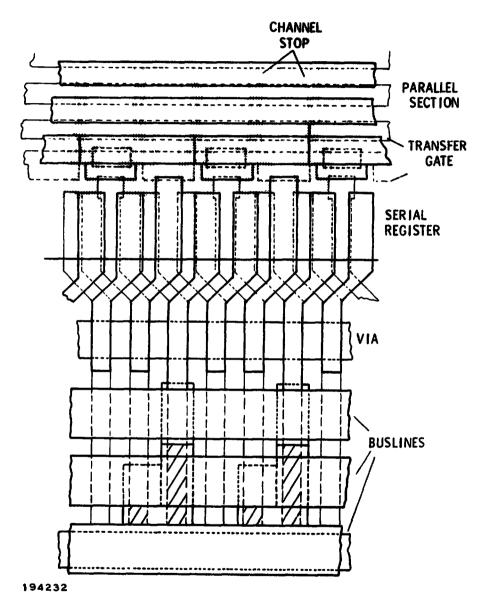


Figure 2-5. Schematic of the 3¢ Interconnection Between Parallel and Serial Registers



that is, a bus at each side of the parallel section is used to allow electrical contact to all electrodes even if there is a break in one of the parallel electrodes somewhere in the array. As a result, all metal is anodized.

The 400 X 400 array was designed using essentially the same concepts as discussed above for the 160 X 100. There were, however, two points of departure—the first being that the BSHA and CCA amplifiers on the 160 X 100 chip were replaced by precharge outputs (Section 1.C.). The second unique feature of the 400 X 400 array is that the parallel section of the area is divided into four 100 X 400 sections by electrically isolating these sections on the array. Thus, there are ϕ_1 , ϕ_2 , ϕ_3 bond pads for each section. All four ϕ_N leads can be joined externally to operate the full 400 X 400 elements or each section could be driven independently to lower the load presented by the array to the driving circuitry. The main motivation for the splitting was that in the event of a fatal defect in one section, the remaining sections can still be operated to obtain an increased number of operating CCDs to evaluate process variables and for other experimental purposes. If the sections are labeled A B C D, as in Figure 2-6, several possibilities would be: fatal defect in A would allow 120 K imager; fatal defect in C and D would allow 80 K imager operating with top serial register, etc.

One technique of achieving an 800 X 800 size CCD array would be to use four operational 400 X 400's in a mosaic. While this would yield a considerable insensitive area if four devices were mosaiced without further processing, the 'dead' area could be reduced considerably if each 400 X 400 was sawed close to two sides of the array as shown in Figure 2-6. To allow this possibility without further redesign of the array, all necessary bond pads to operate the array are positioned on two sides of the array (top and right side in Figure 2-6). A mosaic would now have 5 to 10 percent of its area insensitive to optical input. In the mosaic the readout direction of each array will not be identical but this should not be a particular problem. The problems will appear in thinning each individual array with a 5 to 6 mil thick supporting strip along the two sawed sides of the individuals.

A correlated clamp amplifier; similar in design to the CCA on the 100 X 160, is provided at the lower corner of the silicon chip for use with the 400 X 400. The input to this amplifier can be externally bonded to the video output of the normally used precharge output to obtain a clamped output directly from the chip. This amplifier has not been bonded in the arrays delivered to JPL.

The serial-parallel-serial structure is used for the 400 X 400. This provides valuable redundancy if a defect exists in the lower output serial register since the array can be operated in the reverse direction using the upper register as a readout register. In fact, this is the main function of the upper register since buried-channel arrays do not require injection of any fat zero bias.

The parallel imagining section of the 400 X 400 has 120! electrodes (400 1/3 pixels) and the serial registers have 1203 electrodes (401 pixels). The dimensions of the active area is 360 X 360 mils and the array is fabricated on a silicon chip measuring 500 X 500 mils. Bond pads are approximately 50 mils away from the edges of the main array to allow about a 25 mil region outside this area to be thinned while the bond pads remain on the thick silicon rim. The oversize thinning window is required for good uniformity of the thin membrane over the light-sensitive area of the imager. A photomicrograph of the 400 X 400 is given in Figure 2-7. The implementation of the design discussed above is shown at higher magnification in Figure 2-8. The

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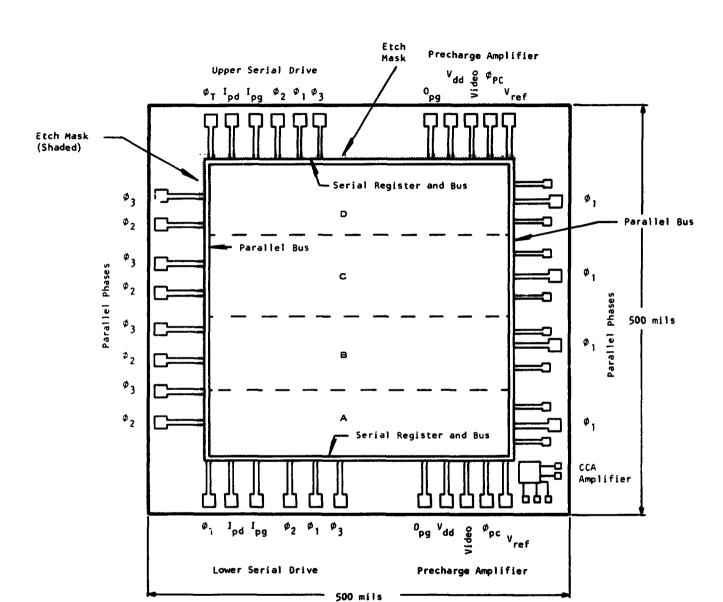


Figure 2-6. Schematic of 400 X 400 Showing All Necessary Bond Pads on Two Sides so that Chip can be Sectioned for Mosaic





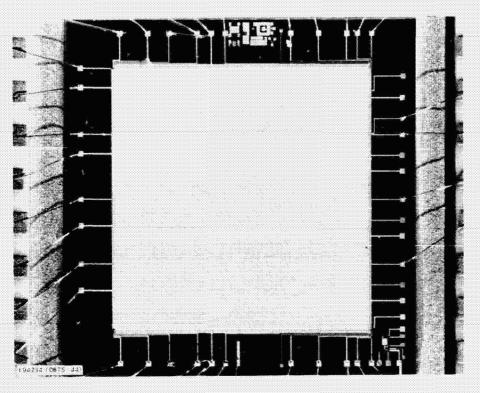


Figure 2-7. Photomicrograph of the 400 X 400 Imager

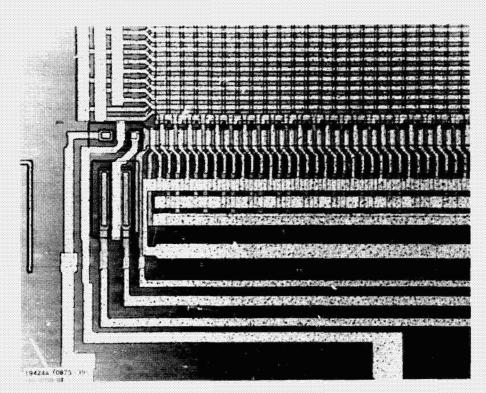


Figure 2-8. De ail of the Parallel-to-Serial Region of the 400 X 400 Showing the Precharge Amplifier Output



contrast in color in this photograph between adjacent electrodes is due to the Al₂O₃ layer on the first metal level.

Experience with the small array indicated that a failure mode often observed was related to metal lead breakage in the region of the via connection (Figure 2-5) where each level should exactly overlap. Dimensional variations in photomasks often led to slight misplacement of these with respect to each other with resulting undercut by the second-level etch. Thus, the second-level electrode in this region was widened by 0.05 mil on each side to overlap the 0.3 mil, first-level lead. This provided improved reliability in this area and the change was incorporated into the 400 X 400 and, later, into redesign of the 100 X 160.

High charge-transfer efficiency CCDs were achieved by using phosphorus ion implantation to achieve a 0.5 to 1.0 μ m deep buried channel in nominally 10 to 15 Ω cm p-type silicon. Typical arrays operated at 6- to 12-volt clocks with a CTE of \geq 0.9999 (measured in the serial register) with no intentionally introduced fat zero. Equally good parallel CTE is inferred from the square wave amplitude response data discussed below. Injection of electrical input at the top serial register confirm the high parallel CTE. The uniformly high resolution of the 400 X 400's is extremely good and reflects excellent buried-channel operation. Consistent achievement of high CTE requires tight control over substrate resistivity and implant dose to achieve the desired channel. Any metalization defects also degrade CTE from the optimum.

B. PHOTOMASK FABRICATION

The design features described above must be transferred to working photomasks to allow device processing. The steps involved in this transformation are discussed in some detail in Appendix H. For the 100 X 160, a 2.5-inch-square reticle is generated, then reduced by a 5X high quality lens to form the final array dimensions. This array is then stepped to form the master photomask. Working photomasks are contact printed from the master to define the geometry on the masks. Twenty-five arrays appear on each photomask of which 18-20 can be used in 2-inch silicon slice processing. A total of nine photolithographic steps are required for the CCD process and exact registration of each level is required for high performance arrays. An additional mask was designed to allow protection of the output amplifier from the buried-channel implant. The function of each mask level is

- 1. Moat definition-p+ channel stops and array isolation
- 2. n+ diffusion
- Contact windows to n⁺
- 4. Contact windows to n⁺
- 5. First-level metal
- 6. Via
- 7. Bus cut
- 8. Second-level metal
- 9. Protective oxide removal on bond pads

Each level defines geometry which is transferred onto the silicon slice in a conventional contact alignment tower.



Particularly tight tolerances are required on the masks to maintain the design electrode overlap of 0.05 mil. Also, overlap of serial electrodes with the p⁺ regions are necessary to avoid gaps which could limit buried-channel operation. This overlap is also 0.05 mil. For the small 100 X 160 it is possible to achieve the required overlap tolerances in the processed CCD with a reasonable degree of care in processing. Very high performance 100 X 160's made at the end of the program confirm that the technology of photomask fabrication is sufficient to realize optimum performance from the 100 X 160 imager when using 2-inch processing.

Initial 400 X 400's were processed on 2-inch silicon which required 2.5 inch square photomasks. Problems of obtaining defect-free geometry, particularly in the channel stop and metal electrode photomasks, were magnified considerably by the increase of 10X in the area which contained the fine geometry. Two types of dimensional variability of the array as it appears on the master photomask and, hence, the working copies, are observed. These are dimension differences between each array on any given mask level and also between the array levels. These changes result from small differences at the step and repeat camera (Appendix H). Absolute positioning of the array on the masks by this camera is subject to a random (mechanical) error. Maintaining absolute positional accuracy for a 2.5-inch-square mask containing nine arrays is effected by runout errors and these are more significant for larger masks, e.g., the 4-inch-square masks used for 3-inch silicon slice processing. The large area of fine geometry in each 400 X 400 is subject to the presence of defects which, for example, join two adjacent electrodes on a metal level or block a parallel channel by allowing the p⁺/thick field in the narrow channel stops to bridge the channel. Hand correction of the reticle (5X larger than the final array) is performed to eliminate most of the defects. Similar work is carried out on the reduced arrays but this cannot be done readily because of the smaller size. As a result, the working masks have some remaining defects and further selection is made in the CRL processing area so that the sets of masks with the lowest defect density are used for slice processing. By using considerable care in processing, it was possible to fabricate the six bars on a 2-inch slice so that all electrodes overlapped as was intended. Alignment markers at each corner of all arrays on the photomasks allow rapid alignment of a level to the previous geometry on the silicon slice but in most cases the final alignment must be done by using the fine geometry features of the arrays themselves.

During the program, processing on 3-inch-diameter silicon was performed. As indicated above, this requires masks to be fabricated on 4-inch glass plates with each mask now containing 25 arrays. Since 21 of these can be used on the 3-inch silicon slice for processing, the requirements on perfection are still more difficult to achieve. It is impossible to achieve 100 percent perfection and at least some of the 21 arrays will fail due to photomask defects. Nevertheless, the number of potentially good arrays which can be processed per slice is significantly greater on the 3-inch material.

Microscopic inspection of photomasks for defects is even more important and more tedious than on the smaller masks. Nevertheless, it is necessary for the lowest defect density in the various process steps.

C. ON-CHIP AMPLIFIER DESIGN

Two different amplifiers have been used on the 100 X 160 imager. The amplifier at the output of the lower serial register is a balanced sample and hold (BSHA) while the upper serial



register output is from a correlated clamping amplifier (CCA). Design of the on-chip electronics assumed that the array would normally be operated in the forward direction (BSHA output) and the CCA design would provide both redundancy and information on low-noise, on-chip processing. Operation of these two circuits is discussed below.

Because of the experience gained from the 100 X 160 array, a decision was made to replace the BSHA and CCA with two simple precharge outputs. This latter configuration does not require as many MOSFETs and was expected to provide somewhat greater reliability in fabrication and operation. This is an important advantage because of the size of the main array and the expected incidence of defects in the parallel section. A second advantage in removing the on-chip load MOSFETs was that the high on-chip power dissipation in both CCA and BSHA caused appreciable heating of thin membrane near the output corners of the array. This will be discussed in a later section of this report.

1. Operation of Balanced Sample-and-Hold Circuit

A schematic of this circuit is shown in Figure 2-9 and a photomicrograph in Figure 2-10. The odd-numbered MOSFETs form one complete sample-and-hold circuit, and the even-numbered MOSFETs another. The circuits are laid out on the CCD chips as mirror images of each other to produce the most balanced responses possible. The input to one circuit is the output diode of the CCD. The input to the other is a nearby floating diffusion designed to have essentially the same impedance as the CCD output diode, and thus should have practically the same response to capacitively coupled and radiated clock feedthrough transients. The advantage

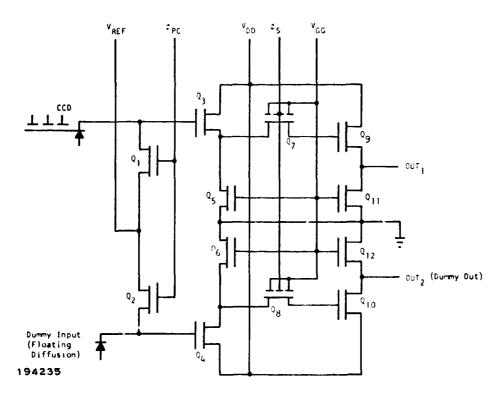
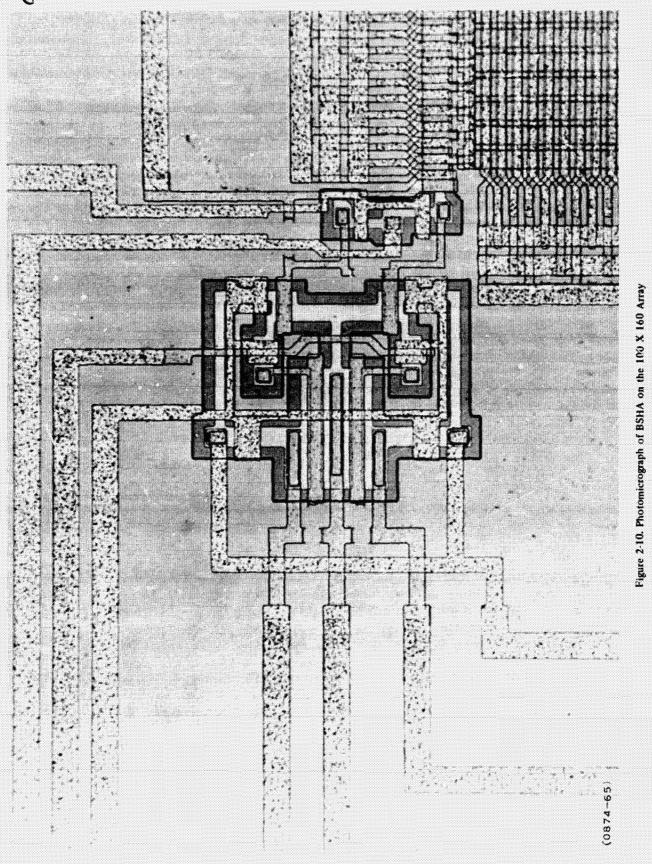


Figure 2-9. Schematic of Balanced Sample and Hold On-Chip Preamplifier







of this technique⁹ has been noted in a recent article on noise from buried-channel CCDs. Outputs of the two balanced circuits may be connected to inputs of a differential amplifier, removing most of the clock feedthrough noise commonly present in CCD output signals.

Operation of the half-circuit connected to the CCD is described below; operation of the other half will be identical, the function of MOSFET number N, where N is odd, being the same as that of number N + 1. To begin one clock cycle, Q1 is pulsed on momentarily to precharge the output diode of the CCD to V_{REI} . Q3 functions as a source-follower, with Q5 its load device. Q7 is the sampling gate, which at this time is held off. Q9 functions as the output source-follower, with Q11 its load device. Sampled information is stored on the gate capacitance of Q9. After Q1 has returned to its off state, the CCD is clocked to dump the next signal charge packet onto the output diode of the CCD, causing a voltage swing on the gate of Q3 proportional to the quantity of charge in the packet. This voltage is followed by the source of Q3 and is applied to the left-hand diffusion of Q7. After this voltage has stabilized, Q7 is pulsed on momentarily, charging the gate of Q9 to the same voltage. Q7 then remains in the off state until the next clock cycle, holding the signal voltage out of the circuit at a constant level.

In actual implementation of the circuit, the gate of Q7 is fabricated as an overlapping three-gate structure, using the double-level anodized aluminum process. Only the center one of these three gates is pulsed; the other two are biased to an on state by applying the voltage, V_{GG} . This arrangement reduces capacitive feedthrough of the sample pulse into the output signal.

The sensitivity of the amplifier operating in the surface-channel mode is about $0.5 \,\mu\text{V/electron}$.

2. Operation of Correlated Clamping Circuit

A schematic of the correlated clamping circuit is shown in Figure 2-11 and a photomicrograph of the device in Figure 2-12. The purpose of this circuit is to reduce the magnitude of "kTC" noise introduced at the output of the CCD, that is, noise resulting from the uncertainty in the voltage level to which the output diode of the CCD may be precharged prior to the arrival of a signal charge packet. The circuit function is based on the common television circuitry concept of dc restoration, whereby an ac-coupled signal is periodically "restored," or clamped, to a dc referenced voltage. The clamping operation consists of charging the coupling capacitor to a voltage which is the difference between the dc reference voltage and the input voltage applied to the capacitor. The noise introduced by the dc restoration process is just the uncertainty in the voltage to which a capacitance C may be preset, namely, $\sqrt{kT/C}$.

Use of dc restoration to reduce output noise in a CCD depends on performing the clamping operation in synchronization with the pulse sequence used to precharge the output diode of the CCD. Referring to Figure 2-11, MOSFET Q1 is pulsed on momentarily, presetting the CCD output diode to $V_{REF} + \Delta V_1$, where ΔV_1 is the deviation of the voltage from V_{REF} resulting from kTC noise on the precharge operation. Q2 acts as a source-follower, with Q3 its load device. Once Q1 has returned to its off state, the clamp gate Q4 is pulsed on momentarily, charging the coupling capacitor C to a voltage V_C . If we assume for simplicity that the threshold voltage of Q2 is zero and that the Q2-Q3 source-follower has unity gain, then V_C will be given by



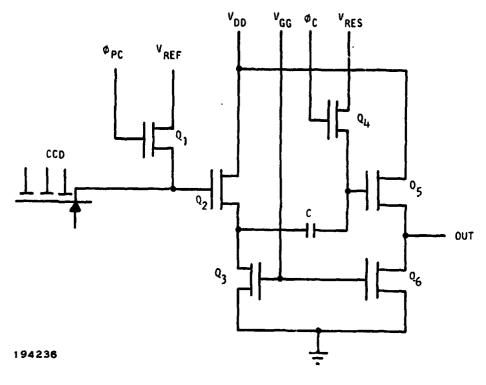


Figure 2-11. Schematic of Correlated Clamp Preamplifier

$$V_C = V_{REF} + \Delta V_1 - V_{RES} - \Delta V_2$$

where ΔV_2 is the deviation from V_{RES} of the voltage on the gate of Q5 resulting from kTC noise on the operation of charging capacitor C. MOSFET Q5 functions as a source-follower with load device Q6. If its threshold voltage is assumed to be zero and gain of the combination to be unity, the output voltage after clamping will be $V_{RES} + \Delta V_2$, independent of ΔV_1 .

If now the CCD is clocked to dump the next signal charge packet onto the output diode, voltage on the gate (and source) of Q2 will change by a voltage ΔV_S proportional to the magnitude of the charge in the packet. As Q4 is now off, the voltage across C must remain at V_C , so the gate (and source) of Q5 also change by ΔV_S . The final output, voltage is thus $V_{RES} + \Delta V_2 + \Delta V_S$, independent of ΔV_1 . Noise on the output signal is the runs fluctuation in ΔV_2 , namely, $\sqrt{kT/C}$. Noise introduced by the output diode precharge operation is the rms fluctuation in ΔV_1 , namely $\sqrt{kT/C_o}$, where C_o is the parasitic capacitance of the output diode mode. This component of noise is completely removed by the clamp circuit, so the noise voltage is reduced by the factor of $\sqrt{C_o/C}$.

In actual implementation of the circuit on the CCD chip, C_0 is approximately 0.25 pF and C is approximately 25 pF, resulting in a noise voltage reduction by a factor of 10. In terms of absolute noise voltage, the rms kTC noise voltage on a 25-pF capacitor is approximately 13 μ V. In terms of effective rms number of noise electrons at the output of the CCD, the noise resulting from the clamping procedure is approximately 20 electrons.

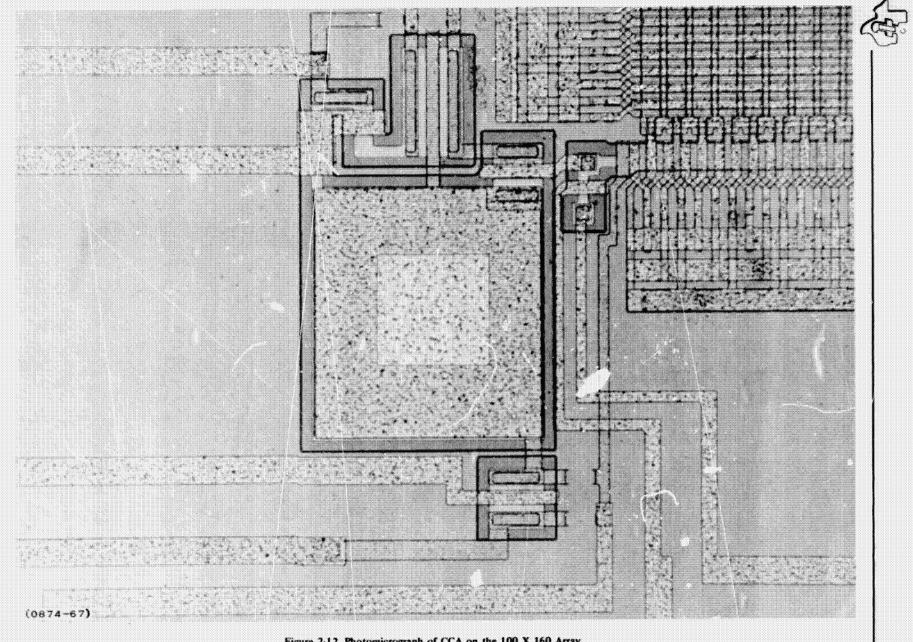


Figure 2-12. Photomicrograph of CCA on the 100 X 160 Array



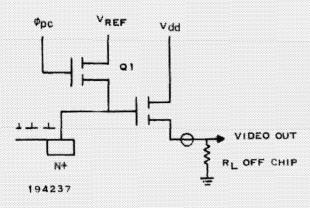


Figure 2-13. Schematic of Precharge Output on the 400 X 400 Imager

3. Precharge Amplifier

A schematic of the precharge output used on the 400 X 400 is shown in Figure 2-13 (see also Figure 2-7). The output diode of the CCD is connected directly to the gate of a source-follower MOSFET. Video output is taken directly from the source and an external load resistor (typically 4.7 kilohms) is connected between source and ground. The output node is precharged to a voltage close to V_{REF} by turning on Q1 with a precharge pulse of ϕ_{PC} . When ϕ_{PC} is removed, the voltage at the gate of Q2 falls to a new level, V_{REF} V_{C} = V due to the gate-source

capacitance of Q2. Charge appears at the fall of the ϕ_2 pulse on the CCD register and appears as a further decrease in the voltage level, V, at the follower gate.

The sensitivity of this precharge amplifier is about $0.50 \,\mu\text{V/electron}$.



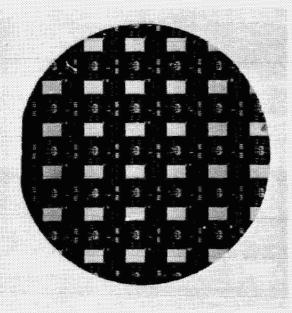
SECTION III CCD FABRICATION

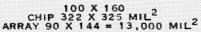
A. DEVICE PROCESSING

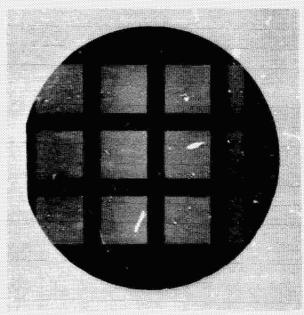
The 100 X 160 CCD arrays were processed in a dedicated MOS processing facility in the Central Research Laboratory (CRL). This area fabricates CCDs only and uses silicon slices of 2-inch diameter. The normal number of devices processed on each 2-inch slice is about 18. A processed "lot" generally contained 10 to 12 slices.

The 400 X 400 array is also processed in CRL using the same MOS process; seven devices are processed on each slice (Figure 3-1). To increase the throughput of the 400 X 400, some processing was carried out on a 3-inch silicon MOS line outside of CRL. Correct design of the masks used for 3-inch processing allowed 23 devices on each slice. Two 3-inch 20-slice lots were processed in this facility during this part of the contract. Because of the location of the 3-inch processing, the process used for the 3-inch slices differed in several small details from that used in 2-inch processing. Differences in device operating characteristics will be discussed in Section VI. The n-channel process used is summarized below and some of the steps are shown schematically in Figure 3-2.

 Initial oxidation and silicon nitride deposition. This forms the mask for steps 2 through 4 in the self-aligned thick-field process.





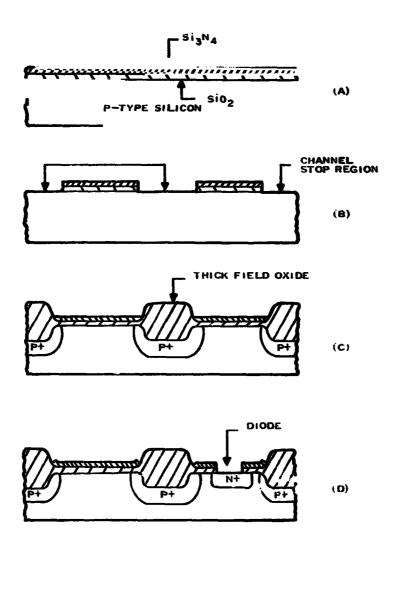


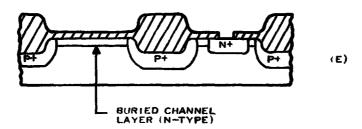
400 X 400 CHIP 497 X 497 MIL² ARRAY 360 X 360 = 130,000 MIL²

194238

Figure 3-1, 100 X 160 and 490 X 400 Processed Arrays on 2-In. Silicon Slices







194739

Figure 3-2. Schematic of Several Processing Steps Used in CCD Fabrication



- 2. Definition of light-sensitive channels in parallel section—p⁺ boron diffusion in channel stops and area outside array
- 3. Field oxidation-thick oxide over p+
- 4. Phosphorus diffusion (n⁺) for diodes and MOSFETs
- 5. Nitride removal and gate oxidation over CCD channels
- 6. Phosphorus ion implant and drive to form buried n-layer for buried channel
- 7. Phosphosilicate glass (PSG) stabilization
- 8. Contact windows to n+
- 9. First level aluminum deposition and definition
- 10. Via mask to protect areas from anodization
- 11. Anodization of metal and subsequent bus cut to isolate metalization
- 12. Second-level aluminum and definition
- 13. Protective Si₃ N₄ overcoat layer.

Also included are bulk gettering processes to reduce impurity concentration and so enhance bulk minority carrier lifetime. This step is essential if low dark current imagers are to be fabricated, especially if they are buried-channel CCDs. The processes used by Texas Instruments are such that at the end of this program a dark current density of less than 1 nA/cm² was measured in a 400 X 400 area imager. The results will be discussed in a later section in more detail.

Many of the parameters involved in the CCD process, such as boron and phosphorus dopant concentration, diffusion conditions, and metal layer thicknesses, have been well determined and at the end of the program were not subject to significant change in slice processing. A considerable amount of study was devoted to optimum gate oxide growth. The present CCD process uses a wet/dry oxidation cycle. The use of this gate with the bulk gettering technique has resulted to date in the lowest dark current devices. Optimum buried-channel parameters to obtain good array operation were more difficult to determine because, while the other steps followed conventional MOS processing, the implant for the buried-channel had to be determined (as outlined in Section IV) and then implanted. The conditions for optimum implant, as judged by charge transport with high CTE, were determined during the 100 X 160 CCD development phase of the program. Of particular importance was the magnitude of the dark current observed in early buried-channel devices. This dark current was high (>50 nA/cm²) and arose predominantly from bulk generation centers in the silicon. Bulk gettering techniques described below were essential in reducing the density of these centers.

To determine the phosphorus concentration necessary to form the thin ($\sim 1 \mu m$) n-layer at the surface of the p-silicon substrate, it is necessary to calculate potential profiles in the CCD. These potential profiles are determined by the doping concentrations in the n and p regions, the CCD electrode geometry and bias voltages applied to the electrodes, buried n-layer via n⁺ diffusions and substrate. In addition to determining n-dopant concentration required, the results allow determination of optimum clock voltages and bias voltages for operation of the CCD in the buried-channel mode together with the distribution of signal charge in the buried channel. These calculations are presented in Section IV.



In both 100 X 160 and 400 X 400 an implant mask was designed to allow the array to be implanted but to protect the amplifier MOSFETs on CCA and BSHA so they remained surface channel. However, in all cases the reset MOSFET was implanted. Generally, the amplifier MOSFETs were processed as surface channel to allow operation at lower $V_{\rm dd}$ than is possible with buried-channel MOSFETs. It appears, however, that a B.C. MOSFET is characterized by lower dynamic noise than an S.C. MOSFET and also that the B.C. device is more resistant to ionizing radiation, such as gamma rays. These advantages probably outweigh that of operating the CCD at a lower $V_{\rm dd}$ (20 to 24 volts versus 30 to 30 volts, respectively).

For several slices of processed 160 X 100 devices, measurements were taken of the turnoff voltage of a test MOSFET across the slice. Generally, across a 2-inch-diameter slice, a variation of about 1 to 3 percent was observed in V_T . This indicates the uniformity of the implant. Test MOSFETs were about 320 mils apart in this test and the results suggest that the implant will be quite uniform across the active area of a 400 X 400 (360 mil²). No effects in the 400 X 400 were seen to suggest that performance was limited by nonuniformities in implant. Also, the best 400 X 400's showed excellent CTE across the array, which, while not being a sensitive function of V_T uniformity, does indicate that if any effect exists, it is not of importance. The high parallel and serial CTE is also evidence for the correct buried channel operating mode.

Even if the device is implanted correctly, poor CTE can result from broken metalization leads. In the initial phase of the program, it was often observed that some of the metal electrodes in the serial register were broken at the place where first- and second-level metal were crossed (Figure 3-3). This was investigated by using a scanning electron microscope (SEM) in the voltage contrast mode. In these measurements, ac voltages are applied to the CCD electrodes while the device is under observation in the SEM. Contrast due to differences in the energy of secondaries, generated at metal with and without voltage, allows the direct observation of a broken bus line since the voltage is not applied to it or to electrodes beyond the break as shown in Figure 3-3. The SEM is particularly valuable in determining failure points and the 400 X 400 design incorporated a somewhat wider second level electrode where it overlaps the vias on first level. This modification appears to stop breaks in the metal which SEM investigation showed to be higher than expected. Definition of etched metal edges is readily observed and allowed development of optimum sloping sides on the aluminum electrodes. An additional problem located by the SEM was cracking of the silicon nitride mask during the thick-field oxidation preferentially around the edges of the channel stop. This is avoided by optimum processing with the nitride mask and is an important consideration because of the rather narrow adjacent transfer gate region between parallel and serial registers.





COLOR CONTRAST INDICATES THAT THE PARTICULAR PART OF THE SUBSEQUENT METAL BUS LINE IS BROKEN SO LINE AND ELECTRODES APPEAR DARK

194240

Figure 3-3. Voltage Contrast Mode of Operation for a CCD on a Scanning Electron Microscope

As indicated in Section II the arrays were designed with 0.05 mil overlap of first- and second-level electrodes. While it is difficult to transfer this to a working photomask, it is even more difficult to transfer this design overlap to an etched metal pattern because of defects in photoresist and undercut by the TIL metal etch used to define the electrode geometry. Great advances in metal etching technique were made during this program.

Each slice is done separately and continually evaluated during the cycle. Undercutting by the etch of the resist pattern is minimal 0.02 mil or less. The design of an additional photomask, which has an oversize electrode structure with 0.42 mil fingers and 0.18 gaps allows a second coat of resist and second etching to open any metal bridging that may remain after defining the first-level electrodes. This technique relies on the fact that a random mask defect in the first photomask will be very unlikely to overlay exactly with a defect on the second oversize mask. It is essential that the second mask be oversized to ensure protection of the already defined electrodes across the total 400 X 400 bar because of errors in photomask registration across the bar. It is very difficult to apply this technique for a second etch of the second level metal because the design gaps are already only 0.2 mil, requiring that the second mask have about 0.1 mil gaps.



B. FAILURE MODES FOR CCD IMAGERS

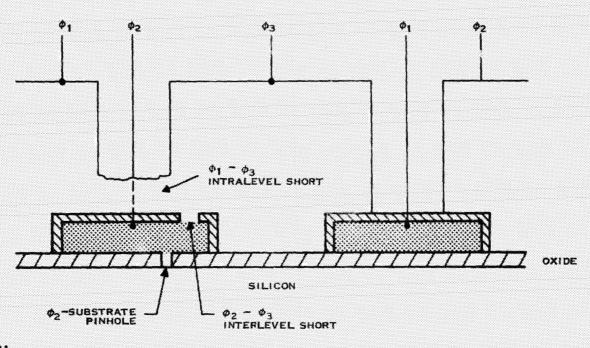
After fabrication is complete, the devices on each slice are tested by a dc multiprobe (HSM) which applies test voltages to the bond pads, detects any accidental electrical connections and provides a computer printout of the failure and its position. For example, ϕ_1 may be connected to ϕ_2 or an n^+p diode may be showing 1 mA of reverse leakage, etc.

The two most important failure mechanisms for the 3ϕ , double-level CCD are interlevel and intralevel metal shorts and pinholes in the gate oxide. These are indicated schematically in Figure 3-4. Because of the four-segment design of the 400 X 400 which allowed arrays between 40,000 and 160,000 pixels to be tested independently for pinholes and metal shorts, data can be obtained on the area dependence of the defects. Data included the 16K 100 X 160 array and a smaller 64 X 64 array. The results can be given in a purely relative sense since any MOS yield data is proprietary. The loss due to pinholes increases with array area approximately as (area) $^{0.3}$ over the range 0.02 to 0.83 cm 2 . Metal loss increases approximately as (area) $^{1-8}$ over the range 0.083 to 0.83 cm 2 .

Due to the design of a 3-phase, double-level CCD (Figure 2-1), the adjacent electrode fingers on each metal level are driven by different clock phases. Thus, bridging of two electrodes joins ϕ_n to ϕ_{n+1} and, since every fourth electrode is electrically connected, results in very poor charge transport. Thus, intralevel shorts are fatal. Interlevel shorts, due to pinholes in the anodically formed Al_2O_3 which insulates first and second metal levels, also occur. The Al_2O_3 is about 2500 Å in thickness and is characterized by about 1 pinhole/cm². Cleanliness during the chemical anodization process is essential for the lowest pinhole density. Since certain areas on the first level metal pattern are covered with resist (from the via photomask) to prevent anodization, it is essential that this via process step does not accidently put resist in the center of the array which must be totally anodized. If a central part of the array is covered it will not anodize (Figure 3-5) and will result in an interlevel short when the second metal level is deposited. Considerable care must be excercised at this point of the process.

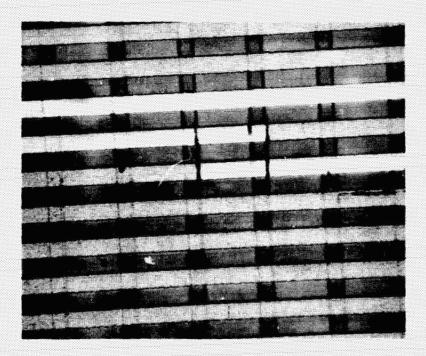
Several techniques were investigated to improve the dielectric integrity of the interelectrode insulation. These included deposition of a second insulating layer, either plasma-deposited Al₂O₃ or Si₃N₄ over the anodic layer. Measurements of the effects of these layers generally suggested lower pinhole density but difficulties were encountered because the additional films were deposited both on the anodic Al₂O₃ and on the gate oxide exposed between the first-level electrodes. This resulted in electrical gate instabilities, high fixed charge and interface state density; therefore, the multilayer approach was not pursued. Comparisons made at Texas Instruments of interelectrode isolation formed by anodized aluminum and by SiO₂ on polysilicon electrodes did not indicate any significant differences.





194241

Figure 3-4. Interlevel, Intralevel, and Pinholes That Form the Failure Modes for the Double-Level Imager



194242

Figure 3-5. Micrograph of an Anodized Aluminum First Level Electrode Structure Showing an Area That Failed to Anodize Because of Particle or Resist Contamination at the Via Process



As discussed above, it is not possible to determine by electrical probing between clock phases after fabrication, whether interlevel or intralevel shorts are the dominant failure mode. It cannot be electrically determined whether shorts occur after first-level patterning because all metal is connected prior to anodization. For the 400 X 400's, many devices were inspected in detail through a microscope to determine the effectivenss of the etching. It appeared that many bars could be made completely free of metal bridges which would give intralevel shorting. While bridging was clearly visible after first-level patterning, the metal bridges could not be visibly detected as easily after the second-level patterning. This seems due to lack of optical contrast between anodized and unanodized levels after second-level etch. These metal defects are the dominant failure mode for 400 X 400 arrays.

The second failure mode is pinholes in gate oxide. These result in connection of phase electrodes to substrate and, if numerous enough, also show as metal shorts because two pinholes can connect two phase electrodes via the substrate (Figure 3-4). "Small" pinholes resulting in a lower phase to substrate resistance than would be normally observed ($\sim 10^5$ ohms versus $> 10^6$ ohms) are often not fatal, provided the load presented by the CCD to the parallel phase drivers is not excessive.

As indicated earlier, the loss due to gate oxide pinholes does not increase directly as the area of gate oxide covered with metal but at a slower rate. This suggests that the pinholes in the best oxides are of sufficiently low density that the smaller arrays do not "see" all the defects on the slice. Some defects giving rise to pinholes may result from nonrandom damage on the slice itself—either from water residue or careless handling in the process.

It is possible that local regions of low dielectric strength in the gate oxides generate white defects in the monitor display from the CCD. While it was originally considered that a positively biased gate would remove electrons from a CCD well through such a "defect" and result in a "black" defect in the display from the device, it has been suggested that such a gate pinhole can show as a white defect. The mechanism, however, for this to occur is not clear. It has been observed that some white defects generated by the application of higher than normal clock voltage, which appear as intermittent white lines in the direction of the (parallel) charge read out, can be permanently "burned" into the CCD signature. If this is done, the white line defect will be present at all clock voltages. Since this defect seems to be related to oxide breakdown, it may support the mechanism above.

However, this effect is not generally observed when the CCD is operated at normal clock voltages and the bulk of white video defects seems material related. Problems relating to the oxide integrity will clearly be more important as the size of the active area increases. For example, the de leakage current measured from the 100 X 160 phases to substrate is always 106 to 107 ohms, while in the 400 X 400, measured resistance is often somewhat lower in some array sections. While device operation is not immediately affected, some "weak" spots in tiese large gate oxide areas probably occur and these probably will ultimately determine the CCD operating lifetime. However, once a 400 X 400 has been determined to operate and image, we have observed no sudden failures due to oxide pinholes, provided that no higher than normal voltage spikes are applied across the gate.



During the course of the program, several techniques were explored to improve the dielectric integrity of the SiO₂ used in the CCDs. The dielectric breakdown, fast interface state density at the Si-SiO₂ interface, and pinhole density were reasured on a variety of oxides grown at 950°C to 1,100°C using wet, dry and HCl-doped oxidation environments. A short discussion of these results is presented in Subsection III,C.

The modes discussed above are the most important in determining imager operation. A less important failure mode is that of leaky diodes due to poor n⁺ diffusion. High series resistance is also observed on rare occasions due to inadequate opening of contact windows to the n⁺ regions. Excessive heat treatment after metalization will result in diode failure because the silicon in the n⁺ region is actually slowly removed from the contact to form a silicon-aluminum eutectic. Since the metal is deposited on the CCD using electron beam evaporation, some heat treatment is mandatory and it has been determined that 400° to 450°C for 30 minutes will anneal the e-beam-induced damage in the SiO₂ without destroying the n⁺ areas. If the metal is stripped after sintering, the reaction is observed as a pitting of the contact areas (Figure 3-6).

C. SILICON OXIDE INTEGRITY

A pinhole in the gate oxide is defined as a low-resistance short between a metal phase electrode and silicon substrate through the SiO_2 . If this occurs at or below 10 V across a 1,000 Å oxide (a field of 10^6 V/cm), it is defined as a pinhole. It appears that these regions of low dielectric strength result from particulate contamination during and immediately prior to oxidation. The question of higher electric field breakdown will be one which impacts device lifetime because continued electrical stress on the oxide can result in defect generation either by thermal or electrical mechanisms and resulting device failure.

Dielectric field strength is determined experimentally by forming MOS capacitors on a test slice of silicon oxidized in the desired manner and then applying a ramp voltage between metal and substrate to measure electrical breakdown. A triggering circuit senses the voltage fluctuations across the capacitor which occur prior to catastrophic breakdown of the capacitor and terminates the ramp at a voltage V_p . The metalization is sufficiently thick to avoid self-healing breakdown events so that V_p really reflects the first breakdown event, which would of course be fatal for an operating CCD. This procedure is done on many capacitors and plots made of the number of capacitors which break down in various field ranges. A typical plot of this type for 100 capacitors is shown in A, Figure 3-7. The area of the electrodes was 1.410^{-3} cm². Similar data for electrodes of increasing area are shown in B and C, Figure 3-7. Pinhole density ρ_i (breakdown from: 0 to 10^6 V/cm) is determined from $-\ln P = \rho_1 A$ where P is the probability of breakdown in some electric field interval and A is electrode area. Values of ρ_1 were 0, 0 and 0.65 for the arrays of 1.4×10^{-3} cm², 7.5×10^{-3} cm² and 4.7×10^{-2} cm² area capacitors, respectively. The distribution of breakdowns at higher fields shows increasing width for larger areas. A commonly used definition in evaluating oxide integrity is

 ρ_2 = the number of defects determined by breakdowns <0.8 E_{max}

where $E_{max} = 9.2 \times 10^6$ V/cm is the maximum dielectric strength of SiO₂ above about 800 Å in thickness.



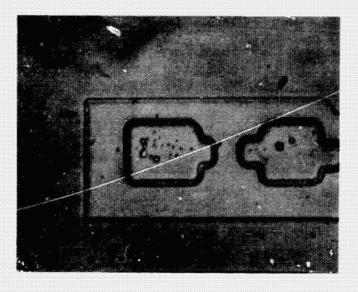


Figure 3-6. Photomicrograph of n^{*} Areas in the CCD Precharge Amplifier Of fined by Removing the Metal Electrodes and Dislocation Etching the Silicon With Section Etch

If ρ_2 is defined as above, values are $\rho_2 = 28$, 18 and 19 for the largest, mid, and small areas, respectively. For a meaningful definition of ρ_2 , ρ_2 should be independent of A but while this is approximately true for low areas it may underestimate ρ_2 for a large contiguous area of oxide as suggested by the data. Estimates of ρ_1 do not scale with area so it is obviously desirable to make measurements using electrode areas simulating the areas of the CCD electrodes. For the 400 X 400, the gate oxide area is $\sim 360 \times 360$ mil and later oxide evaluation work used test capacitors of 300×300 mil.

The use of HCl to improve dielectric integrity has been reported in the literature. A study of the effects of HCl in the O_2 ambient during dry oxidation cycles was made at various oxidation temperatures and HCl concentrations. Values of MOS capacitor storage time τ_s and fast interface state density, N_{ss} , were measured by pulsing an MOS capacitor¹⁰ and using the conductance anomaly [G(V)] technique, respectively. The bulk generation lifetime, τ , can be obtained from the total relaxation time measured after the capacitor has received a voltage step from accumulation into deflection. The relationship of τ_s and τ depends on the magnitude of the step, oxide thickness, and doping density. For the oxides typically used for the following tests (1,200 Å), a 20-volt step and 10 Ω cm material, $\tau = 5 \times 10^{-7} \tau_c$. Thus $\tau = 100$ seconds is equivalent to $\tau_s = 50$ microseconds. The analysis of conductance anomaly to obtain N_{ss} is more complex and was determined by direct computer analysis during the experiments which were performed using metal probes in pressure contact with the aluminum electrode of the capacitor. Variation in defect density ρ_1 and ρ_2 defined above with change in oxidation temperature are



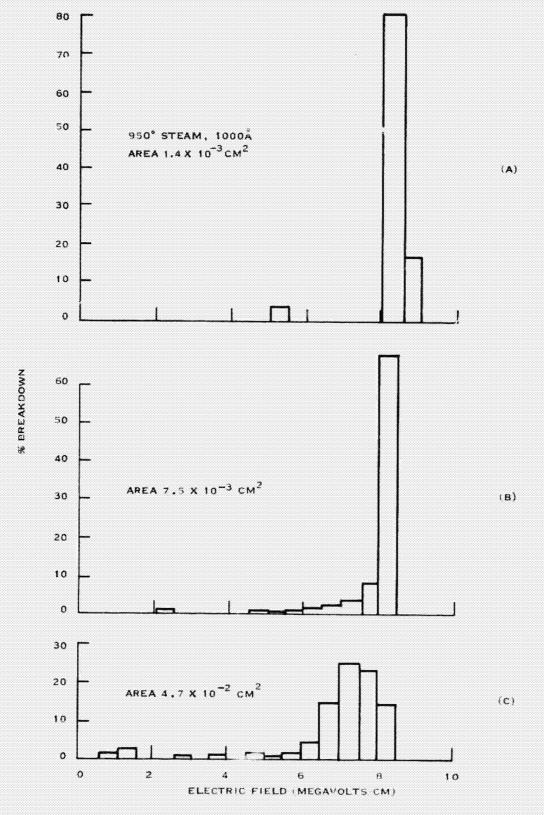


Figure 3-7. Percentage of Capacitors That Break Down at a Field ϵ for Various Area Capacitors on Oxidized Silicon Slice. A "Perfect" Oxide Would Give 100% at the Intrinsic Breakdown on SiO₂ at 9.2 × 10° V/cm. (D) Shows Dependence of ρ_1 and ρ_2 on Oxidation Temperature (Sheet 1 of 2)



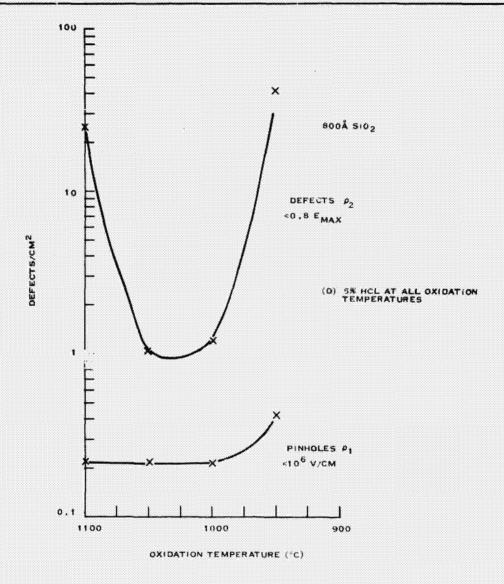


Figure 3-7. Percentage of Capacitors That Break Down at a Field ε for Various Area Capacitors on Oxidized Silicon Slice. A "Perfect" Oxide Would Give 100% at the Intrinsic Breakdown on SiO₂ at 9.2 × 10⁶ V/cm. (D) Shows Dependence on ρ₁ and ρ₂ on Oxidation Temperature (Sheet 2 of 2)

shown in D, Figure 3-7. In all experiments incorporating HCl, an increase in the peak of the breakdown distribution with increasing HCl was observed up to about 5 percent HCl. A representative plot is given in Figure 3-8. There appeared to be very little if any decrease in pinholes with increasing HCl content. Increasing HCl also leads to a reduction in N_{ss} (shown in Figure 3-9), which is more pronounced at an oxidation temperature of 1,100°C than 1,000°C. The beneficial effect of HCl on capacitor storage time, τ_s , is observed for an oxidation temperature of 1,100°C but is not as obvious at 1,000°C.

In the initial phase of the program, devices were processed using HCl-doped oxides and the reduction in dark current was quite dramatic. However, for the imagers, improvements in other



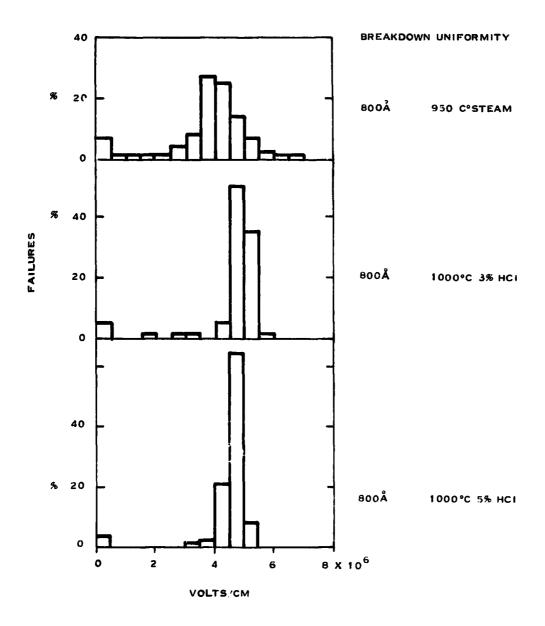


Figure 3-8. Electrical Breakdown of Oxides Containing HCl. Distribution for 1,000°C Oxidation With No HCl is Essentially Identical in this Case to 950°C Steam



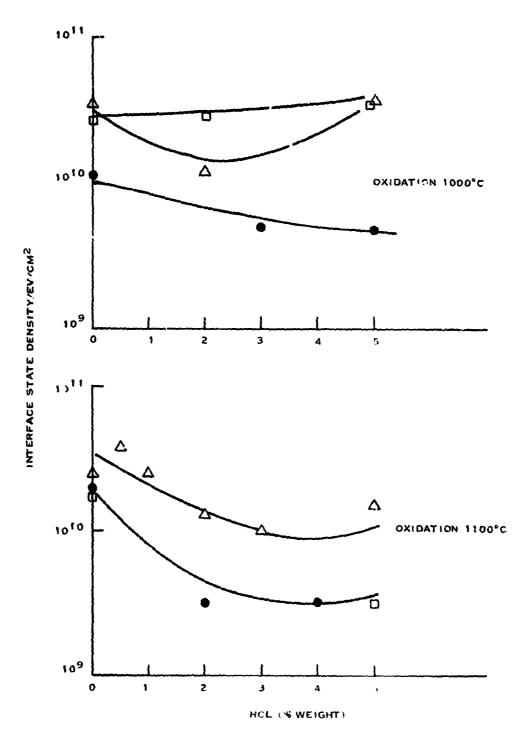


Figure 3-9. Variation of Fast Intefface State Density With HCl Content for 1,100 C and 1,000°C Oxidations



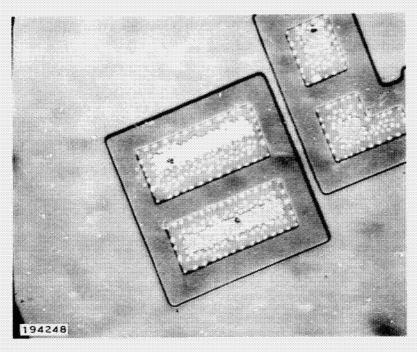


Figure 3-10. Appearance of Spots on n Diffused Areas of CCD With HCl-Doped Gate Oxide

bulk gettering techniques surpassed the improvement from HC1 doping so that present devices do not use these doped oxides but, rather, use a dry-wet oxidation cycle. During these early experiments the CCDs were generally characterized by rather high density of localized dark current spikes and these appeared to be higher than in the "non-HC1" oxides although the background was lower. However, technology has improved considerably and a new comparison would be an interesting speriment. Often in the use of HC1 during oxidation, white spots, shown in a micrograph in Figure 3-10, would appear preferentially on n⁺ diffusions and, to a lesser extent, on the gate oxide itself. These may lead to the dark current spikes and possibly to reliability problems.

The use of HCl as a cleaning ambient prior to oxidation is a well-known procedure used to obtain a clean surface at or above 1.100°C prior to depositing epitaxial layers. Several experiments were carried out to determine if such cleaning at lower temperature could be achieved prior to in situ growth of a gate oxide. The following discussion suggests that such cleaning can improve oxide integrity and also that oxide quality can be degraded by oxide steps (simulating channel stops).

Typically in the CCD process, channel regions (which had been protected with a layer of Si_3N_4) are prepared for oxidation by conventional chemical cleaning techniques. Slices are then spun dry and transferred to the oxidation furnace where they are unloaded from a carrier box and inserted into a quartz holder which is subsequently pushed into the furnace tube. The



quality of the oxide will depend on the surface contaminants present on the slice which can be due to:

Residue on the surface from the original slice polishing process

Localized particulates not removed by chemical cleaning

Nonoptimum removal of the final deionized rinse water (18 megohms)

Particulate contamination from the furnace tube during loading.

To reduce slice contamination prior to oxidation, a number of experiments have been performed using a vapor-cleaning cycle immediately before slice oxidation. The cycle takes place after the slices are loaded and are at the temperature required for oxidation (950° to 1,100°C). At the conclusion of the cycle, which is carried out in an etching ambient, oxidation is initiated immediately by switching to an oxygen or steam-rich gas flow.

Table 3-1 indicates the composition of the initial etching gas and cleaning times for several experiments. Cleaning occurred at the same temperature as the following oxidation. For some of the experiments, the cleaning cycle resulted in the growth of a small amount of oxide, as evidenced by the oxide thickness difference between control slices which had not received the clean cycle and the vapor-cleaned slices. This growth naturally depends quite strongly on the composition of the etching ambient and, by close control of O₂ content, the cleaning cycle can result in either slow oxide growth or slow silicon etching. At 950°C the silicon etching rate for mixtures containing 10 percent HCl is, however, quite small since significant removal does not

TABLE 3-1. INITIAL ETCHING GAS, CLEANING TIMES, AND RESULTS

Run	Cleaning Ambient	Oxidation	Δ in Dielectric Strength (volts/cm)	Δ Pinholes/cm²
229	57 HCl 2% O ₂	5% HCl in O ₂ 1,050 C	5 to 7 × 10 ⁶	0.54 to 0.54
	97% N ₂ 80 mins	900 A to 960 A		
244	10% HCI	steam	3.5 to 6.5 × 10 ⁶	1.6 to 0
	4% O ₂ 86% N ₂ 30 mins	950 C 810 4 to 910 4		
244A	As above but slices ha	d thick oxide ridges	2 to 6 × 106	0.54 to 0.54
276	5% HCl 4% O ₂ 91% N ₂ 30 mins	steam 950 (5.5 to 6.5 × 10°	1.6 to 1.6
301	5% HCl 2% O ₂ 93% N ₂ 30 mins	steam 950 C	2 to about 5 × 10 ⁶ Distribution very wide after cleaning	1.6 to 1.6
360	10% HCl 4% O ₂ 86% N ₂ 30 mins	steam 950 C 1,000 x to 1 230 x	3 6 to 6 × 10 ⁶	0.54 to 0.54



appear to begin below the temperature range 1,050° to 1,100°C. P-type silicon of nominal 2 to 3Ω cm and 7 to 10Ω cm were used. The effectiveness of the vapor clean was measured from the breakdown of an array of MOS capacitors on the slice. Aluminum of about 11,000 Å thickness was evaporated using an e-beam and subsequently etched to give 16 capacitors, each of which was 300 × 300 mil² area. Such large areas are necessary to determine the pinhole density of the SiO₂ which was sufficiently low to be undetectable with more usual size (100-mil dots) test devices. The results are considered more relevant to the determination of potential yield loss from gate pinholes in larger CCD arrays where gate oxide areas are close to 1 cm². Capacitor breakdown was measured by applying a ramp voltage (10 volts/second) to the device and sensing the voltage at which the first fluctuation in the ramp occurred using a triggering circuit. This was taken as the first indication of breakdown at some point in the oxide. Table 3-1 shows the increase in the peak position of the breakdown electric field distribution and pinhole density resulting from several clean cycles. Plots of the number of capacitors which break down in a given electric field range are as shown in Figure 3-11. In this experiment, pinholes are indicated by the events which occur below 5 V/cm. Each set of data presented is the average of two slices. each having 16 test devices. Slice-to-slice variations were always much less than variations which will be presented as evidence of the importance of the particular process variation introduced in the experiment.

Figure 3-11 shows results of experiment 244 using vapor cleaning with 2 to 3 Ω cm material. From A and B, Figure 3-11, it is seen that the cleaning cycle has a significant effect on both pinhole density and dielectric strength. Cleaning has increased the peak of the distribution from about 3.5 × 10⁶ volts/cm to 6 × 10⁶ volts/cm and reduced the pinhole density from 1.6 cm² to 0 (Table 3-1). However, such a dramatic reduction in pinhole density is not typical of our results and, on the average, there is a much smaller reduction. In all experiments performed, however, there was a clear indication of increased dielectric integrity as evidenced by the shift in the maximum of the distribution. Distributions, however, were generally broader after cleaning as indicated in both Figure 3-11 and Figure 3-12. These results suggest that the residual pinholes may be related to material imperfections on the silicon surface which persist through both the chemical and vapor-cleaning cycle. Evidence from CCD area imagers has accumulated to indicate that pinhole defects are not randomly distributed over the slice and this is also suggested by the present results.

In B and C, Figure 3-11, effects of vapor cleaning on slices covered with 0.2-mil-wide thick oxide (10,000 Å) strips separated by 10-mil-wide regions of 1,000 Å gate oxide can be seen. These ridges simulate the channel stop structure of a CCD imager on which gate oxide must be grown. Comparing A with C, Figure 3-11, or B with D, Figure 3-11, effects of these ridges are to broaden the distribution somewhat, an effect which may be due to enhanced breakdown at the thick/thin oxide boundaries. This could result from contamination at these steps which persisted through the cleaning cycle. Development of ultrasonic cleaning techniques, investigated briefly in this program and found to be ineffective on reducing CCD pinhole loss, should probably be investigated further. Comparing C and D, Figure 3-11, the improvement in dielectric strength after vapor cleaning is apparent, while, in this case, the pinhole density remains low and is not decreased.

A and B, Figure 3-12, show results of a similar cleaning cycle on 7 to 10 Ω cm slices as well as the effect of a phosphosilicate glass (PSG) stabilization layer over the oxide (C and D, Figure 3-12). Such layers are routinely used in CCD processing. A 1½-minute deposition (C,



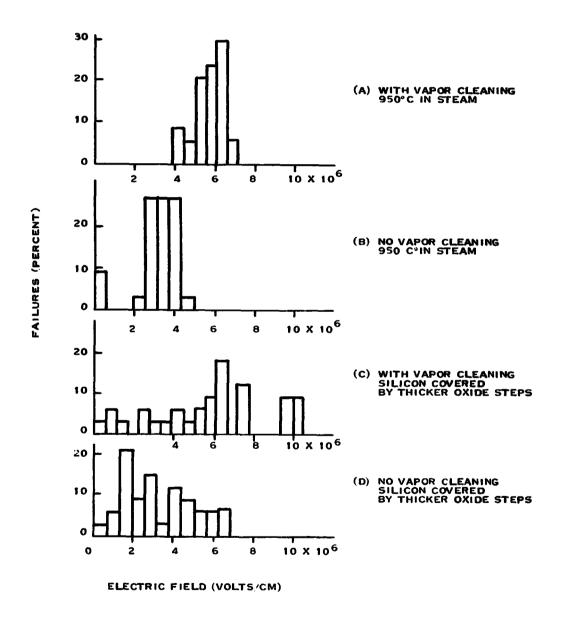


Figure 3-11. Effect of Vapor Cleaning on Oxide Integrity



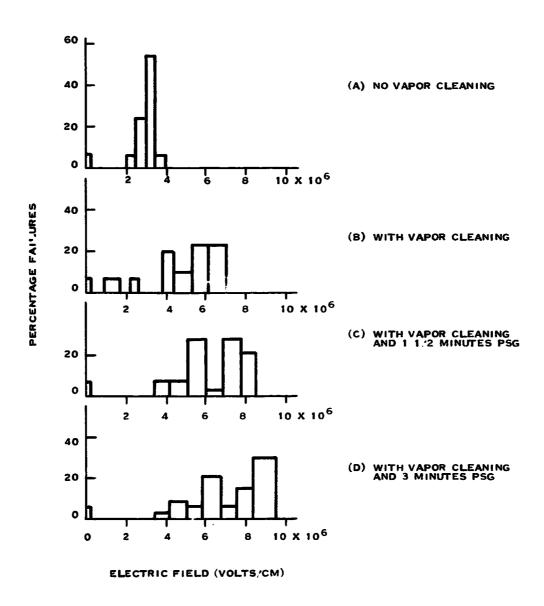


Figure 3-12. Effect of Vapor Cleaning on Breakdown on 7 to 10 Ω cm Silicon (A and B) Addition of PSG Layer Further Increases Strength but Does not Change Pinholes



Figure 3-12) about 50 Å thick shifts the distribution and narrows it. A 3-minute deposition (D, Figure 312) about 80 Å thick further improves strength. The PSG process does not significantly affect pinhole density, a result observed on most high quality oxides. For less perfect oxides (pinhole density 20/cm²), we have observed some decrease in pinhole density after PSG deposition.

Measurements were made on oxides grown after vapor cleaning to determine oxide parameters such as MOS capacitor storage time τ_s , flat-band voltage V_T resulting from the cleaning cycle. N_{ss} was determined to be $1.3 \times 10^{10} / \text{cm}^2/\text{eV}$ in both cases from the conductance anomaly (G/V) technique. MOS capacitor storage time (directly related to bulk lifetime) increases by a factor of 2 after vapor cleaning. We have found similar increases in τ_s by incorporating 4 to 6 percent HCl uniformly into an O_2 stream during 1,100°C dry oxidation cycles. In that case it has also been shown that the chlorine doping also results in higher dielectric strength oxides. Thus the quality of 950°C steam oxide grown after vapor cleaning is enhanced qualitatively in the same manner as observed for the chlorine-doped 1,100°C dry oxide. The lower temperature steam cycle avoids the sometimes undesirable effects of high temperature dry oxidation such as autodoping to adjacent slices.

The improvement in oxide integrity may be due to either an improved silicon surface prior to oxide growth or the incorporation of chlorine, probably in a thin SiO₂ layer at the silicon surface, during the cleaning cycle. Further experiments are required to separate these possibilities. In particular, closer control of the clean cycle ambient so that no oxide is grown prior to steam oxidation is necessary.

However, it should be noted that in the case of dry oxidations with HCl introduced into the O_2 flow during the total oxidation time that the Cl ion concentration is localized at the Si-SiO₂ interface. We suspect that the present oxides also have such a composition due to the particular growth cycle. Since, qualitatively, improvements in oxide integrity are similar in both cases, it is suggested that chlorine doping is responsible for the improvements reported in this note.

D. SILICON PURITY

Fabrication of highly reliable, high-performance charge-coupled device sensors places many stringent requirements on the quality of the starting sill on wafers. In particular, the minority carrier generation rate in the silicon must be minimized to reduce diode leakage and increase charge storage times. Thus, impurities and defects which serve as generation-recombination centers must either be absent in the starting silicon wafers or must be removed during subsequent processing. Also, resistivity variations over the wafer will affect the fixed pattern noise associated with the sensor and influence the implant dose required for the buried channel.

Silicon wafers similar to those requested for CCD processing were supplied by the Chemical Materials Division of Texas Instruments and were used to study residual impurities.

The silicon crystals are dislocation-free Czochralski grown with a specified initial bulk lifetime greater than 50 microseconds. These crystals are grown from polycrystalline silicon having a specified impurity content of less than 0.2 ppb Cu, 10 ppb Na, and 0.002 ppb Au as



established by neutron activation analysis on a random-sampling basis. The radial resistivity variation is not specified. The crystals are then centerless ground and the flats applied. Wafers are cut from the crystal and chemically etched to relieve stresses caused by saw and grinding damage. The wafers are then chemical-mechanical polished to provide a mirror-smooth polished surface, free of damage resulting from slicing operations.

To determine whether impurities were introduced during subsequent processing from the polysilicon up to the polished wafer, a random sampling of polished bulk slices were submitted to neutron-activation analysis with the following results.

Bulk samples, B1-B6, each consisting of two wafers from a specified silicon crystal, were used in the analysis. Samples B1 and B2 were taken from the same crystal and an oxide layer grown on B1 for comparison purposes. These wafers were irradiated in a Union Carbide reactor for 24 hours at 8 × 10¹² neutrons/cm²/sec. After irradiation, all the wafers were rinsed in HCl-methanol to remove surface contamination which might have been introduced during irradiation. Samples B1-B6 were then weighed and their back surfaces masked. The oxide layer was stripped from sample B1, and the sample rinsed. The remaining samples were etched in planar etch for 15 seconds to remove possible surface contamination from handling. Samples B1-B6 were then etched for 2 minutes each in planar etch and the etch solution retained for analysis; the volume of silicon removed was determined by weight difference.

All solutions were analyzed by high resolution Ge(Li) spectroscopy. Detection limits and observed concentrations are given in Table 3-2. For comparison, the results of some polished slices intended for use in standard MOS manufacturing are included.

TABLE 3-2. DETECTED IMPURITY CONCENTRATIONS IN ATOMS/CM³

Samples	Na 1014	Cu 1014	As 1013	Sb 1013	Au 1011
ВІ	5.8				
B2		1.3	2.3		8.2
В3			1.7		3.7
B4	1.9	1.2	1.6		41.0
B5	1.2	0.6			20 0
В6	1.3		2.4		32.0
Limit*	1.0	0.6	1.2	0.8	2.1
Typical polished slice	27	10	180		290

^{*}Interference-free limit for average sample

The conclusion here is that, within the uncertainty of the neutron activation analysis, there is no introduction of Cu into the silicon wafers during the processing from polysilicon. It would appear that there is up to an order of magnitude greater Au in the wafers than specified for the original polysilicon. Note that for sample B1, where the wafer was first oxidized prior to irradiation, the Au content is below detectability.



A second area of starting material evaluation has been wafer surface quality. Several aspects of wafer surface quality (cosmetic defects in or on the wafer surface) have been investigated. It was found that cosmetic quality could best be revealed through visual inspection under a high-intensity white light source (500-watt projection lamp collimated to 2 inch diameter). Inspection under the high-intensity source, however, will even reveal defects too minute to be easily observed in a scanning electron microscope. This high-intensity source has been useful in showing several types of cosmetic defects, including minute silicon particulate contamination, haze associated with the polishing process, and water residue; and an inspection procedure using this source has become a routine part of the slice cleanup procedure in the CRL CCD Processing Facility.

To determine the effects of certain sequences used in the CCD process on the heavy metal impurity content of the silicon slice, neutron activation analysis was performed on test wafers; results of the analysis follow.

Ten silicon samples were irradiated for 14 hours at a flux of 0.98×10^{13} n/cm²/sec at the reactor facility at Texas A&M University. Upon return to TI, the slices were cleaned in HCl:CH₃OH. The oxide was removed from all slices using 10 percent HF. After a deionized water rinse, the first $5.74 \, \mu m$ of the sample were removed for analysis using deionized water planar etch. The thickness of silicon removed was determined by weight difference. For samples 1 and 3, only $4 \, \mu m$ were removed for analysis. These samples were counted 17 hours after irradiation, which gave enhanced sensitivity for 12-hour (half-life) Cu and 15-hour (half-life) Na. All other samples were counted between 24 to 41 hours after irradiation.

The identification of the samples is as follows:

Slice Number		2	3	4	5	6	7	8	9	10
1. Initial oxidation	x	X	X	X	X	X	X	X	x	X
2. Nitride			X	X	X	X	X	X	X	X
3. Gate oxidation			X	X	X	X	X	X	X	X
4. Buried-channel ion implant			X	X	X	X				
5. Implant drive and anneal			X	X	X	X				
6. PSG			X	X	X	X	X	X	X	X

Impurity concentrations in atoms/cm³ and interference-free detection limits for all observed elements are given in Table 3-3. All of the signals observed are close to the detection limits; therefore, errors as high as 50 percent must be assumed. In the absence of any signal, refer to the detection limit. There is some indication of an increase in Au from the starting polycrystalline silicon.

To reduce bulk impurity concentration in the processed silicon slices, a modified phosphorus gettering technique is used in the CCD process. The effectiveness of this cycle was evaluated by using high-resolution gamma-ray spectroscopy to determine levels of N_a , Cu, Au, As, and Sb, both before and after the cycle. Results of the analysis, unfortunately, give concentrations sufficiently near the detection limits of the technique so that clear interpretation is difficult. However, it is possible to measure the minority carrier lifetime, τ , by pulsing an MOS



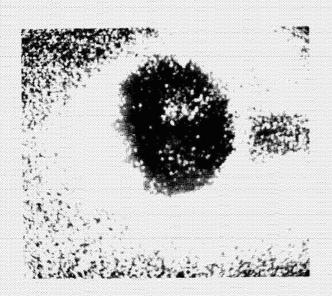
TABLE 3-3. DETECTED IMPURITY CONCENTRATIONS IN ATOMS/CM³

	Na 1014	Cu 1014	As 1013	Sb 1013	Au 1011
Detection Limit	9.5	1.9	0.0	2.8	7
Sample					
1	0.7	0.18	<6.3	<6.0	28
2		<2.5	<5.9	3.8	22
3		<4.4	<9.2	4.1	60
4		<3.3	<8.0	<6.5	8.3
5		<2.9	6.7	<4.6	12
6		<2.2	<5.1	0.59	38

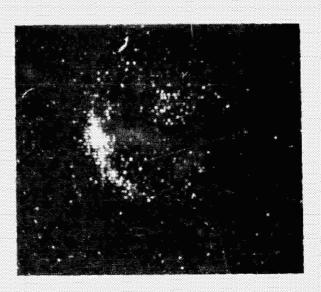
capacitor into depletion; τ is a very sensitive measure of both surface and bulk impurity centers. These measurements indicate significant increases in τ as a result of the modified gettering cycle. Lifetimes of up to 500 microseconds at 24°C have been measured on slices that have been subjected to this cycle, compared to 1 to 10 microseconds on untreated material. The effectiveness of this cycle is superior to formation of oxide using HCl doping which, on the average, increases bulk lifetime of good quality silicon by about a factor of 5. Much more pronounced increases due to HCl can be observed if the initial starting material has lower lifetime. While the modified getter cycle has generally been effective in reducing both overall dark current level and the fixed-pattern noise associated with dark current variations, there still often occur a number of video defects or blemishes which are either not amenable to the modified getter cycle or do not appear to be intrinsic in the silicon. There is evidence that some dark current spikes result from contamination by particulates located in the gate oxide regions of the CCD. One such experiment was performed by ion microprobe analysis of a slice after gate oxidation. A 20 keV O_2^+ beam, focused to about 15 μ m was used to sputter the sample surface. The beam was constantly swept in a 200 X 160 μ m raster to ensure that the inclusion would not be completely sputtered away before the sputtered secondary ion spectrum was recorded. X-Y elemental distribution maps were recorded by preselecting a secondary mass peak and using the ion intensity to modulate the brightness of a CRT whose raster was synchronized with the primary beam raster. Figure 3-13 shows the results of the elemental distributions; the inclusion defect was found to be high in Na, Mg, Ca, and Fe. Intensity area profiles were also recorded by using the secondary ion current to modulate the Y-axis of the CRT. The CRT raster was modified in order to show a projected view of the sample surface. These results are shown in Figure 3-14. Both the X-Y elemental distribution maps and intensity area maps show that the defect impurities are restricted to the actual inclusion. These circular areas are often seen by optical inspection of a processed CCD which has had the gate oxide stripped and then has been etched using a dislocation etch.

A second ion-probe microanalysis of particulate matter found in the gate oxide region after gate oxidation revealed large amounts of Al and Ti with minor amounts of Na and K. The thickness of the particles was in the 1,000 Å to 2,000 Å range. Analysis of the defects suggests that they are related to particulate matter which was present on the wafer before the thermal gate oxidation. The unusual nature of the contamination, Al and Ti, indicates a probable





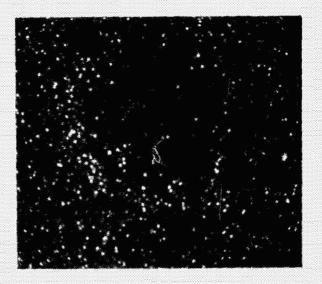
SILICON



ALUMINUM



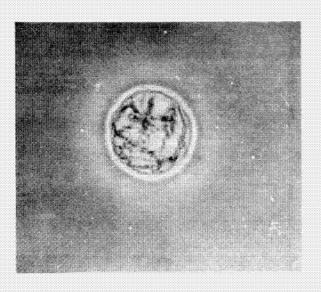
SODIUM



CARBON

Figure 3-13. Elemental Distribution From Ion Microprobe of Several Elements Detected on a CCD (Sheet 1 of 2)







OPTICAL CALCIUM

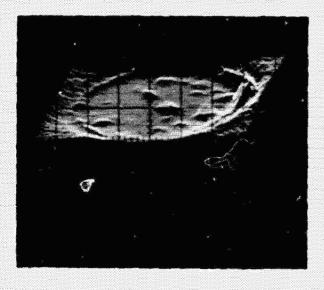




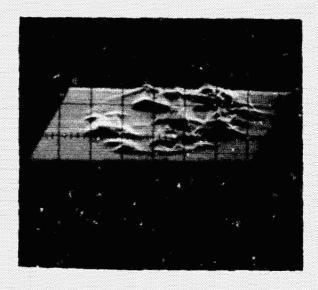
IRON MAGNESIUM

Figure 3-13. Elemental Distribution From Ion Microprobe of Several Elements Detected on a CCD (Sheet 2 of 2)

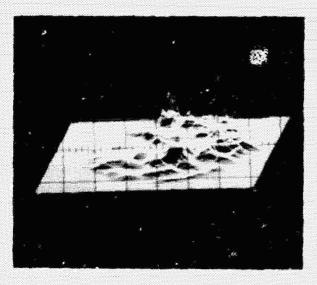




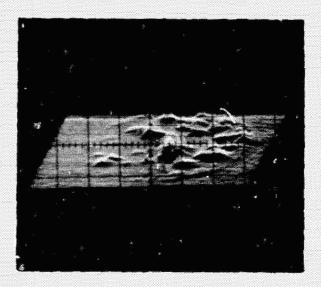
SILICON



CALCIUM



SODIUM



IRON

Figure 3-14. Intensity Profile For Several Elements Detected on the CCD



Al₂O₃-TiO₂ complex such as a pigment in paint. It was also established that the source of one large dark current spike in a CCD shift register was caused by just such an Al-Ti contamination. Such contamination is not routinely observed.

In an attempt to determine other sources of contamination, an ion microprobe scan of the mass 40 peak, either Ca or a silicon-carbon complex, was made in an area which appeared to be characterized by an anomalously high impurity count compared to the rest of the CCD area. A comparison between the areas is shown in Figure 3-15. The contaminated area has a strong localized mass 40 near the oxide-silicon interface while it is not as significant for the five typical areas on the CCD. This probably arises from pregate chemical cleaning contamination.

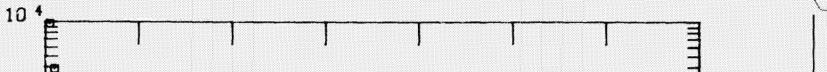
A second mechanism generating white video defects in the output of a CCD imager is dislocations in the silicon, discussed in the following subsection.

E. DEFECT CENTERS IN SILICON

Fabrication of CCD imaging arrays places a more stringent requirement on silicon quality than is normally needed for integrated circuits. While no studies of the effect of silicon material defects on CCD image quality have been presented in the literature, previous work on vidicon camera targets has shown that dislocations, stacking faults, and impurity precipitates can contribute to video defects in a silicon imager. Integrated circuit yield, which, generally, is not directly affected by most preexisting silicon lattice defects, has been shown to decrease substantially as a result of process-induced defects such as stacking faults caused by oxidation, diffusion-induced strain around silicon pitride windows, and thermal strain generation, especially along the periphery of a silicon slice. (Many of these defects have been found to be nucleated from preexisting defects.) Charge-coupled-device imagers combine the high performance requirements of a silicon vidicon with the complex processing of an integrated circuit and, therefore, place the greatest demands upon control of silicon purity and crystalline structure both before and during the device processing.

Silicon material defects can manifest themselves in several types of device degradation. Presently, the most limiting effects are those tied to the role of silicon defects as generation-recombination centers. Such centers generated array dark current. Reductions in dark current and dark-current nonuniformity to the lowest levels will ultimately depend upon identification of the contributing defects and development of process or starting-material modifications. Dark-current spikes or blemishes can be caused by material defects within the device depletion region and, therefore, serve as an excellent means by which to correlate the cause with the effect. Such defects may also be associated with impurity clustering. Such clustering makes it much more difficult to getter the impurity. Examination of the video output of a CCD area array imager provides the exact spatial location of the defect, which can then be compared with structural examination of the underlying silicon in that region.

The technique of reflection and transmission X-ray topograph was used to study the defects. The experimental technique is conventional. X-ray topography has three advantages for the detection of defects over other existing techniques: It is nondestructive, since only λ -rays touch the sample: it is a subsurface technique, which allows defects in the active regions of the CCD to be detected, and considerable information concerning the nature of a defect may be obtained by studying the topographic contrast under different diffracting conditions. In transmission topography, the λ -ray beam passes through the sample, thereby imaging all defects



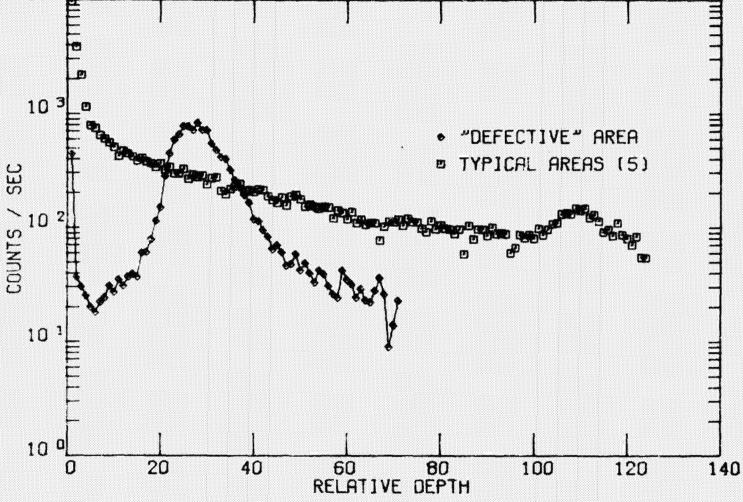


Figure 3-15. Ion Microprobe Signal at Mass 40 as a Function of Depth Into an Oxide-Covered Slice Showing Possible Contamination at the Si-SiO₂ Interface



in the sample. This technique is ideally suited for determining if defects in the bulk cause, or are associated with, defects near the surface. In reflection topography, the diffracted image arises only from the subsurface. The depth to which this image is formed is dependent on the absorption of the beam in the sample, and thus on the incident and reflected angles of the X-rays with respect to the surface, and on the radiation used. For reflection topographs from (111) and (100) slices, the table below lists the depth below which no appreciable contribution to the topographic image is expected.

Reflection	Slice Orientation	Radiation	Image Depth
			7
(224)	(111)	CuKa,	30 µm
(224)	(001)	CuKo,	15 µm
(113)	10011	CuKa,	4 µm

Since reflection topography allows examination of the subsurface region, it is capable of providing information on defects lying ithin the depletion region of the CCD, while the nearest comparable defect-imaging technique, with etching, is capable of revealing only those defects which intersect the surface.

For a device examined in most detail using this technique, a listing of all dark-current spikes was made from the video output by bit and line. These points were then plotted on a transparent overlay so that direct comparison could be made to the X-ray topographic photograph. In cases where a video defect extended over more than one bit, even at low substrate voltages, a point in the center was chosen for the defect site. Although much characterization was done with the device still in its package, topographs were also taken after demounting the device and stripping the metalization and oxides. The outline of the device could still easily be seen from the strain pattern of the diffusions. Because of the curvature of a thin CCD membrane, no useful data was obtained on CCDs after thinning.

Figure 3-16 shows a reflection X-ray topograph of a 100 X 160 device after stripping of the surface oxide and metal films. The faint horizontal lines correspond to strains from the channel stop diffusions. Output amplifiers are clearly visible at the bottom corners of the topograph. B. Figure 3-16, is the same topograph shown with the video dark-current blemish overlay. An almost complete one-to-one correspondence exists between the video pattern and the linear defects that are parallel to channel stops. Cases where the linear defects appear in the topograph with no corresponding blemish in the video overlay were examined in detail. In each case, a blemish that was too faint to be recorded on the overlay was observed. Similarly, blemishes in the video that seemed to have no corresponding defect in the topograph were examined. Again correspondence was found in topographs taken under other diffraction conditions.

The linear defects are shown at higher magnification and under different diffraction conditions in Figure 3-17. This figure shows that the defects appear to emanate from the channel stop diffusion region into a channel region.

The contrast behavior of the linear defects in topographs taken by diffracting from different planes is consistent with the defects being dislocation arrays, with the array possessing a macroscopic strain component in the (110) direction, i.e., perpendicular to the channels evidently intersecting the depletion region, where they act as sources of dark current generation.





Figure 3-16, 422 Reflection Topograph of 100 X 160 Array with Metal and Oxide Stripped. [Arrow is projection of the normal to the (422) planes.] (Sheet 1 of 2)



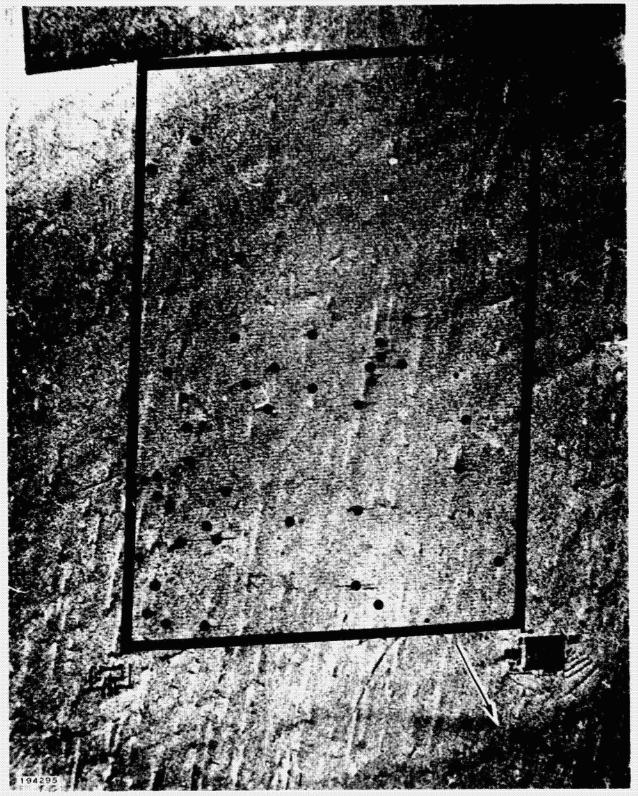
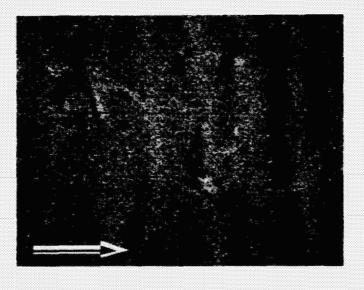
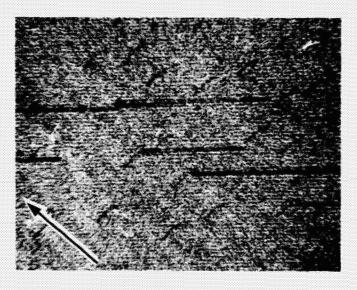


Figure 3-16, 422 Reflection Topograph of 100 X 160 Array with Metal and Oxide Stripped. [Arrow is projection of the normal to the (422) planes.] (Sheet 2 of 2)





(A)



(B)

Figure 3-17. Enlargement of (242) Reflection Topograph of 400 X 250 CCD Array Showing Linear Defects Emanating from the Diffused Channel Stop. Linear Defects Appear to be Nucleated from Other Defects (A): Enlargement of (040) Transmission Topograph of 400 X 250 CCD Array on (100) Material Showing Linear Defects Nucleated from Preexisting Dislocations, Which Lie on Inclined Planes (111) Planes and Pass Through the Wafer (B).



At one end of a linear defect there generally appears to be some other defect (for example, A, Figure 3-17). This is probably the nucleating site for the defect. These, in turn, appear to be associated with the light bands which are nearly parallel to the (110) direction (Figure 3-16). It is obvious that additional characterization of the defects is required. Transmission electron microscopy should furnish more precise information on the nature of the defects, whether or not they cause precipitation, and fill in the picture on how they were formed.

While it is certain that the end points of each linear defect intersect the silicon surface, the dark-current blemish placement is not accurate enough to determine whether the blemish originates at one of these end points. Characterization of devices with better CTE should provide sharper spikes, and possibly answer this question.

Examination of a (100) area array revealed similar linear defects parallel to channel stops. For example, B, Figure 3-17, is a transmission topograph showing linear defects originating from a preexisting dislocation. There were, however, many other types of defects present that have interfered with the preliminary confirmation of correlation with blemishes.

A second experiment was performed using an array which showed the effect of damage inadvertently induced at a cleaning step in the process. This results in dark current defects as indicated in A, Figure 3-18. The X-ray topograph of this device is shown in B. Figure 3-18, where it is possible to identify the heavier dark-current generation sites as regions of darker channels. The point A marked in Figure 3-18 identifies the same corner of the array. However, it was not possible to identify on this device all the defects which were formed in the circular dark-current rings.

The driving force for the appearance of the linear defects is most probably strains in the channel stop arising from the boron diffusion and the edges of the overlying oxide. The sense of these strains is in the (110) direction. These strains are relieved during high temperature processing by the introduction of dislocation arrays. The particular role played by each processing step is not yet understood. It should be noted that the channel stop region undergoes stress reversals during some of the process steps.

The role of the crystallographic orientation of the slice on defect formation appears mainly to determine the length of the linear defects. With a (111) slice, the maximum resolved shear stress on any slip system is twice that in a (100) slice for oxide window/boron diffusion stresses. However, with the channel stops oriented in a (112) direction on a (111) slice, no (111) slip planes are parallel to the channel stop, and a dislocation array can grow down the channel stop only by a cross-slip/climb mechanism, which is thermally activated. On the other hand, in a (100) slice, the array can propagate along a (011) direction by glide which is a much easier way, hence the linear defect is longer.

Interestingly, a (110) slice orientation with channels in a (001) direction would seem to be the best to minimize the size of the linear defects. This orientation would have maximum resolved shear stress identical to the (100) slice orientation, but, since the channels are not parallel to (111) planes, the dislocation array could propagate only by the cross-slip climb mechanism. Dislocations can also be shown by simple techniques of dislocation etching a CCD which has had both the metalization and SiO₂ removed. Figure 3-19 shows the results of a Secco dislocation etch¹⁷ on a processed 400 X 400 CCD indicating the linear dislocations both parallel and perpendicular to the narrower channel stop region. Oxidation of the silicon in these regions in the CCD process grows about 14,000 Å of SiO₂ in these regions and this allows the



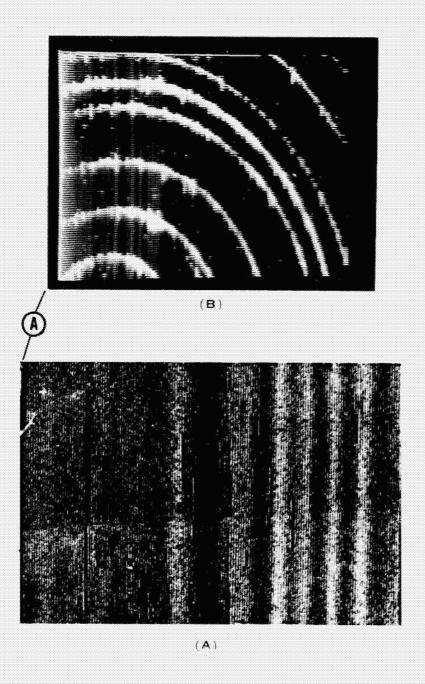


Figure 3-18. X-ray Topograph of 100 X 160 CCD Imager (A) and Video Output from the Device Showing Damage (B)





Figure 3-19. Dislocation-Etched CCD Obtained After Stripping Metal and Oxide Showing Dislocation Grown in the Thick Oxide Channel Stop Regions

dislocations to grow so they are readily observed. The channel area (wider in Figure 3-19) does not undergo this oxidation, therefore defects in the silicon are not as readily observed. A correlation of these etch-identified defect regions with CCD performance has not been made on a point-by-point basis. It appears, however, that higher density of such defects is correlated with lower level optical performance on the CCD array. These defects are not caused solely by the p⁺ and thick oxide process itself because they are not always present in etched devices processed with nominally identical p⁺ and thick oxide parameters. Even across a given CCD active area there is often a wide spread in defect density. These observations suggest that the defects are present in the original silicon or are introduced by a random (and unidentified) variation in one of the processing steps.

F. THINNING AND BACKSIDE ACCUMULATION

The CCD is fabricated on a standard silicon wafer of about 16-mil thickness. In a backside-illuminated mode, optimum CCD resolution and short wavelength response require that the silicon directly over the light sensitive area of the CCD be thinned to a thickness in the range of 10 to 12 μ m. An area slightly bigger than the array itself is thinned to avoid nonuniformities at the thick-to-thin silicon edge affecting device performance. Membrane stability is such that repeated cycling from 24° to -40°C does not fracture the CCD. Initial thinning of the whole silicon slice to about 8 mils is done either mechanically or chemically. Further thinning down to



final thickness can be performed using either of several techniques. In all methods described below, the thinning process is monitored by a combination of time and visual inspection by transmitted light at the edges of the array metalization. The color of the membrane is very sensitive to the silicon thickness.

During initial thinning work for this program the unthinned 8-mil CCD chip was first mounted in a ceramic header (described in the following subsection) using a low-temperature setting epoxy. The header was encapsulated in a Teflon holder, leaving the back surface of the CCD exposed. The assembly was then etched in the rotating beaker. This technique resulted in nonuniformities and excessive surface staining of the thinned membrane. The etch solution could also leak between the silicon chip and the header surface around to the electrode side of the CCD with fatal results.

An improvement in thinning resulted from etching the thinning windows for all devices on a slice simultaneously. This is referred to as whole-slice window thinning.

Rectangular thinning windows with a dimension of 170 × 120 mils, providing ~30 mils between the 144- by 90-mil active area of the 100 × 160 were used initially. With this design rather uneven etching and some residue on the final membrane were often observed. As a result of this, a circular thinning window of 0.21-inch diameter was designed. This resulted in all features of the array being clearly visible using transmitted light and also gave improved etching uniformity around the window edges due to improved fluid flow around the recess. The final surface of the thin CCD is generally shiny although some surface haze is often present. This is thought to be residue from the etch cycle and is variable from device to device over a slice and from slice to slice. However, by careful attention to several critical steps in the cycle, a surface of uniform, stain-free quality is achieved. Figure 3-20 shows a slice of 100 × 160 arrays after window thinning.

A third technique, referred to as chip thinning, involves scribing and breaking the slices which have been thinned to 8 mils, then selecting only devices which are defect-tree for further thinning.

Since there is often a variation in etching rate across a slice and it therefore becomes difficult to obtain uniform membrane thickness for all devices when the whole-slice window thinning is used, the chip thinning offers some advantage in the fact that a single device can be optimally thinned.

Both techniques, whole-slice window and chip-thinned 100 X 160's have been successfully applied and there is no clear advantages seen at present to either technique.



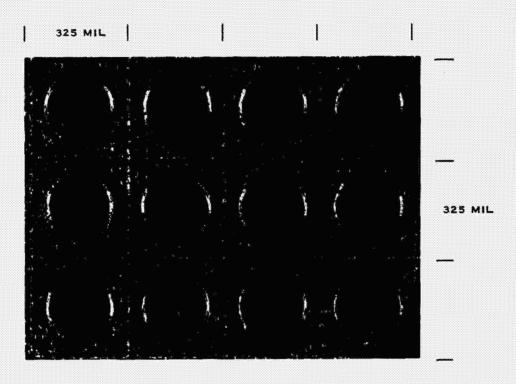


Figure 3-20. Portion of a Thinned Silicon Slice Containing 100 X 160 Arrays Using Whole-Slice Thinning

The thinning technique used on initial 400 X 400's was whole-slice window thinning with excellent results. The area to be thinned is now square and measures 410 X 410 mil, leaving a thin transparent region about 25 mils wide at each side of the array. The array can sometimes be misaligned with respect to the thinning window by misplacement of the mask defining the windows. This is because the alignment is done using a low-power infrared microscope with illumination beneath the silicon. Improved magnification would allow improved alignment.

With the use of 3-inch silicon slices for the 400 X 400 the number of bars increased to 21 from the 6 on each 2-inch slice. Whole-slice window thinning is still adequate but due to the increased volume of silicon to be removed, increased etch volume is required if the etch is not to be depleted and cause irregularities. For this reason chip thinning is often used—especially if there are only a small number of good arrays on the slice. Front and back views of thinned 100 X 160 and 400 X 400 CCD imagers are shown in Figure 3-21.

Membrane thickness is typically in the 10 to $12 \,\mu m$ range. Thickness uniformity is rather variable depending on the particular device selected. The uniformity is conveniently measured by illuminating a CCD imager with narrowband 10,000 Å illumination and observing the interference fringes from the video monitor display. The difference in membrane thickness, Δd is given by

 $\Delta d = 1/2 \text{ n } \lambda$



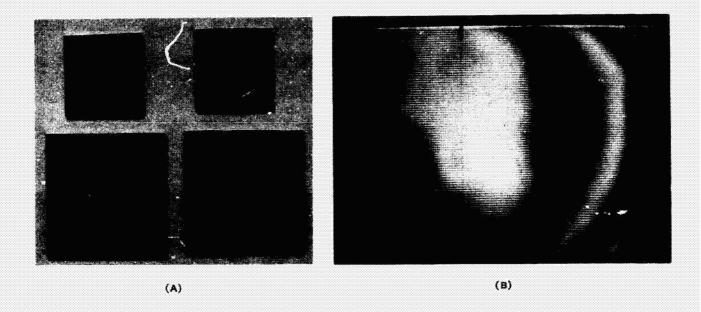


Figure 3-21. Back Side and Front Side of Thinned 100 X 160 and 400 X 400 CCD Imagers. In (B) the Interference Pattern from a 100 X 160 Array Illuminated with 10,000 A is Shown.

where

n = 3.42 is the refractive index of silicon

 λ = the wavelength of the incident light.

Uniformity is generally $\lesssim 0.5 \,\mu m$ for the 100 X 160 imagers. A representative fringe pattern is shown in Figure 3-21.

The backside surface of the thinned CCD imagers is accumulated to provide a drift electric field in the silicon to sweep minority carriers, photogenerated at the backside surface, into the CCD depletion wells. This increases short wavelength optical response. Backside surface resistivity measurements indicate that boron accumulation of 10¹⁷ /cm³ over the bulk doping level of 10¹⁵ /cm³ can be achieved using proprietary Texas Instruments techniques. The process is, however, rather variable from device to device in the extent to which 4000 Å response is increased. Values of quantum efficiency of 65 percent at 4000 Å have been achieved, although more typical values are somewhat below this value.



G. HEADER DEVELOPMENT

The header structure for the 100 X 160 arrays is a 40-lead edge card, nominally 2 by 1 by 0.040 inches, fabricated from 95 percent alumina. A 0.25-inch-diameter bevelled hole, located at the center of the CCD chip mounting area was cut into the header by means of an ultrasonic abrasion technique. This allows incident optical radiation to be focused on the backside of the CCD. Details of etch thinning a CCD after it was mounted in this header to achieve the desired, approximately 10-µm membrane over the active area was quite dependent on fluid flow patterns around the edges in this 40-mil hole. The chip is mounted in the header using a thin line of room-temperature-curing epoxy between ceramic and chip. This method of mounting has been found to be completely effective in providing a mechanical bond with the CCD operating over

the range -40° to $+40^{\circ}$ C and avoids the high temperatures which would be involved in alloying the chip to the header. This temperature cycle (to about 400°C) can lead to increased warping of the thin membrane. Figure 3-22 is a photograph showing the front view of the header after mounting the CCD chip. Connections are made from 8- by 8-mil bond pads on the CCD chip to gold metalized leads on the header by conventional ball bonding with 0.8 mil-diameter gold wire. Pin connections to the card are listed in Table 3-4. Pin 1 is at the left-hand edge of the card as viewed in Figure 2-22. Representative operating voltages for buriedchannel imagers are given in parentheses in Table 3-4.

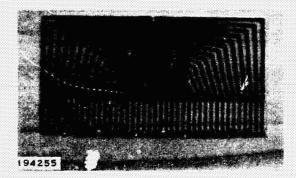


Figure 3-22. Mounted 100 X 160 CCD in 40-Bin Edge Card

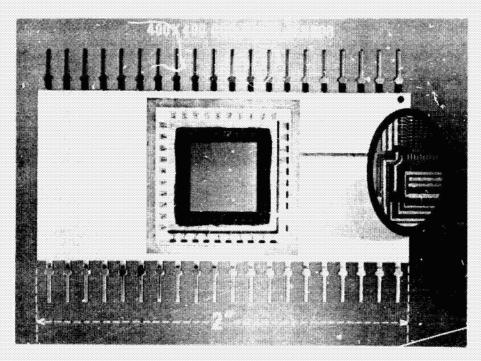
The 400 X 400 arrays were mounted in a ceramic 40-pin dual in-line package designed for the array. It is 2 inches in length and the pins are 1.0 inch apart. A hole in the ceramic of 420 X 420 mil was provided to allow light to fall on the sensitive area of the CCD. Most chips were epoxy mounted. Several chips were alloyed to the chip at higher temperatures to see if the membrane warped excessively. By careful alloying at each corner of the array, no excessive warpage was seen and in some cases the membrane appeared even less deformed after alloying than after epoxying. A photograph of a 400 X 400 mounted in the DIP header is shown in Figure 3-23 as viewed from front and back showing the thinning window. As above, connections were made to the CCD bond pads with 0.8 mil gold wire. Pin connections to the DIP are given in Table 3-5. Pin 1 is identified by a locating dot on the ceramic and pin 21 is directly opposite pin 20 across the short dimension of the header. Electrical pin connections for the 400 X 400 are given in Table 3-5. For the 400 X 400 there are four sections, each 100 X 400, which can be operated independently. Thus, there are four connections for each parallel phase. As indicated earlier in Figure 2-6, these sections are defined as A, B, C, and D. By connecting all four together, the array will operate normally.



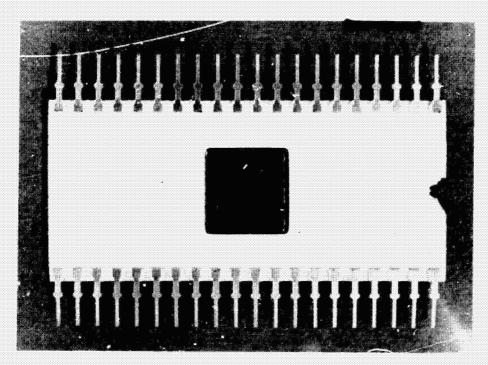
TABLE 3-4. 40-PIN EDGE CARD, PIN CONNECTIONS FOR 100 X 160 (ADVANCED) (Typical Buried-Chan .: Operating Voltages in Parentheses)

de	1	Substrate 0 to -5 V (-2 V)
pulse	2	φ upper serial phase +5 V to +15 V (+8 V)
pulse	3	ϕ_s^* upper serial phase +5 V to +15 V (+8 V)
pulse	4	φ [*] upper serial phase +5 V to +15 V (+8 V)
	5	No connection.
	6	No connection.
de	7	l_{pg} input gate, upper serial connect to ϕ_i^*
dc	8	I _{pd} input diode, upper serial 0 - 25 V (25 V)
pulse	9	$\phi_{ m T}'$ transfer gate upper serial to parallel. (Same voltage as ϕ_1' , ϕ_2' , ϕ_3')
pulse	10	φ' ₃ parallel phase +5 V to +16 V (+8 V)
pulse	11	ϕ_2' parallel phase +5 V to +16 V (+8 V)
pulse	12	ϕ_1' parallel phase +5 V to +16 V (+8 V)
pulse	13	$\phi_{ m T}^{\prime\prime}$ transfer gate, parallel to lower serial. (Same voltage as $\phi_{ m T}^{\prime}$)
dc	14	I _{pd} input diode, lower serial 0 - 25 V (25 V)
	15	No connection.
	16	No connection.
pulse	17	I_{pg} input gate, lower serial connect to ϕ_1
pulse	18	φ ₂ lower serial phase +5 V to +15 V (+10 V)
pulse	19	ϕ_3 lower serial phase +5 V to +15 V (+10 V)
pulse	20	ϕ_1 lower serial phase +5 V to +15 V (+10 V)
dc	21	Opg lower serial output gate 0 to +10 V (+3 V)
pulse	22	ϕ_{pc} precharge pulse (BSHA) overlap of ϕ_1 and ϕ_2 (18 V)
pulse	23	$\phi_{\rm S}$ sample gate (BSHA) from leading edge of $\phi_{\rm I}$, width ~80 ns, (+15 V)
dc	24	V _{ref} precharge reference voltage (BSHA) 0 to +20 V (15 V)
	25	No connection.
	26	No connection.
	27	Vgg load bias (BSHA and CCA) 0 to +20 V (+15 V)
	28	Dummy video output.
	29	Video output
	30	Ground
de	31	V _{dd} drain voltage (BSHA and CCA 0 to 25 V (+24 V)
	32	Output video 2 (CCA)
	33	V _s source bias for load MOSFETs (CCA) (grounded)
pulse	34	$\phi_{\rm C}$ clamp pulse (CCA) 80 ns pulse. Triggered positive edge of $\phi_{\rm S}$ (+15 V)
	3.5	No connection.
	36	No connection.
đ¢	37	V _{res} voltage on clamp drain (CCA) 0 to +20 V (+15 V)
dc	38	Opg upper serial output gate 0 to +10 V (+3 V)
pulse	39	$\phi_{\rm pc}$ precharge pulse (CCA) 0 to +20 V overlap of ϕ_1 and ϕ_2 (+15 V)
de	40	V _{ref} precharge reference voltage (CCA) 0 to +20 V (+15 V)





(A) FRONT



(B) BACKSIDE

Figure 3-23, 40-Pin Dual In-Line Header for the 400 X 400 Imager



H. CCD DRIVE ELECTRONICS

Electronic circuitry used to drive the 100 X 160 and 400 X 400 arrays consists of a timed sequence of pulses to transfer charge and to operate the on-chip preamplifiers. Operation at any

TABLE 3-5, 40 PIN DIF PIN CONNECTIONS FOR 409 X 400 (Typical voltages as in Table 3-4)

1	oʻ,	parallel phase Section B			
2	φ' ₃ parallel phase Section C				
3	oʻ.	parallel phase Section D			
4	No connect	connection			
5		o connection			
6	V _{ref}	upper serial output amplifier			
7	Ģ ķ	apper serial output amplifier			
8	Video	upper serial output amplifier			
y	Vad	upper serial output amplifier			
10	O_{0u}	output gate upper serial			
11	o, t	upper serial			
12	No connec	tion			
13	ϕ_i^*	upper serial			
14	6,1	upper serial			
15	lnd	mpor diode opper serial			
16	91	transfer gate upper serial to parallel			
17	at,	parallel phase Section D			
18	a',	paraflel phase Section D			
19	ψ',	parallel phase Section C			
20	ø',	parallel phase Section C			
21	ϕ_i	parallel phase Section B			
22	<i>i</i> .	parallel phase Section B			
23	ď,	parallel phase Section A			
24	ωţ	parallel phase Section A			
25	្ស	transfer gate parallel to lower serial			
26	l _{ist}	input diode fower serial			
27	ð,	lower serial			
28		lower serial			
29	34,	lower serial			
3 ()	Substrate				
31	O_{pg}	output gate lower serrat			
32	V _{dd}	lower serial or (put amplifier			
33	Spc. 7	lower serial output amplifier			
34	Viet 5	lower secols, aput amplifier			
35	No connect	tion y			
36	No connect	ion			
37	No connect	liog			
38	No connection				
19	No connect	ion			
40	e),	purallel phase Section A			



data rate from 10 kHz to 3 MHz is possible and at any integration time. The format for the tests made under this contract is listed for each of the characterization tests that are listed in Appendixes of this report.

The sequence of clocking pulses generated and applied to the CCD electrodes is indicated schematically in Figure 3-24. The pulse sequence for the output signal processing is shown in Figure 3-25 on an expanded time scale. The CCD output shift register is designed so that the last phase electrode prior to the output gate in ϕ_2 . The signal charge is thus dumped, via the de-biased transfer gate, on the output diode diffusion at the fall of ϕ_2 . Excessive clock feedt trough to the video waveform has been observed on occasion due to preamplifier related defects but, generally, does not occur. The first electrode in the serial register is, therefore, on ϕ_3 to make 160 pixels. Transfer of charge from the last electrode in the parallel section of the array (ϕ_1 parallel) occurs through a composite transfer gate into ϕ_3 serial. The timing diagram (Figure 2-19) shows both ϕ_2 and ϕ_3 (serial) held high at this time. This is the situation on the test setup to allow other CCDs to operate correctly but only ϕ_3 need be high for the line scanner design. The precharge is held high during flyback to allow the first bit on each line to be transferred correctly.

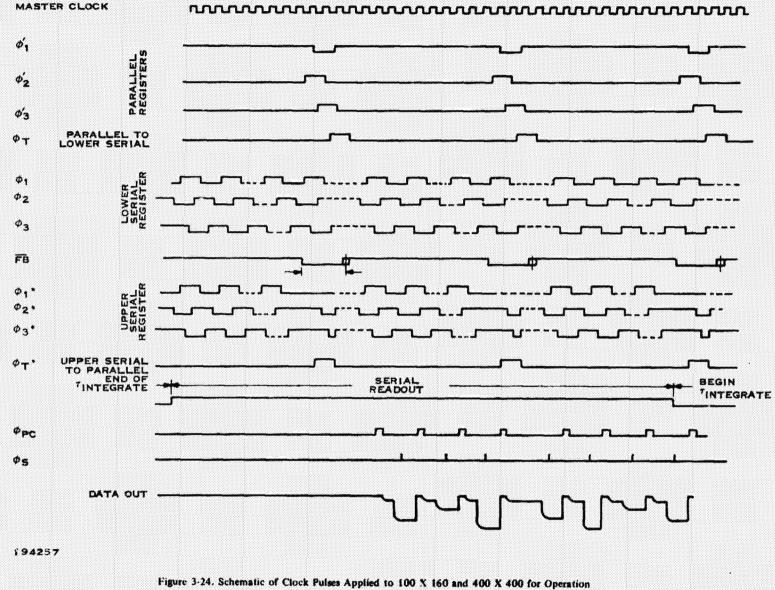
Typical operating potentials and pulsewidth information is given in Table 3-4. The CCD array is operated in the reverse direction by switching ϕ_1 and ϕ_2 in the parallel section and interchanging the clocks between the two serial registers. This is necessary since the upper register clock waveforms are modified to allow injection of (fat zero) change to the parallel section as shown in Figure 3-24.

By applying a dc potential to the sampling gate (ϕ_7) of the BSHA, a percharge output can be obtained from the chip. The video output is then affected by the less-than-unity gain of two source followers. Output from the CCA appears as a precharge waveform (Figure 5-3) but the level prior to the output signal should be clamped at some dc level. Preliminary evaluation of the CCA showed a bandwic: of about 1 MHz compared to 7 MHz for the BSHA. The stability of the clamp level was often not adequate and the amplifier itself appeared to be more subject to processing-induced failure than the BSHA. Further work is needed to optimize the CCA on-chip circuit.

The load presented by the CCD to the driving electronics can distort the "ideal" pulse shapes delivered by the circuitry. For the 100 X 160, the capacitance between a given phase and substrate is about 500 pF. There is also several hundred picofatads between ϕ_N and ϕ_{N+1} due to overlap of electrodes and coupling via the depleted buried in layer. For the 400 X 400, the capacitance is several thousand picofatads per phase. The effects of such a 400 X 400 load on the serial and parallel phase drivers is shown in Figure 3-26 for 1 MHz data rate (from serial) and in Figure 3-27 for a 16 kHz data rate. These waveforms were observed at the CCD pins, which are in the low-temperature Dewar at the end of about 18 inches of cable connected to the drivers themselves. Placing the drivers at the CCD would decrease the effects observed at the rise and fall times. Clock feedthrough, due to coupling between ϕ_N , ϕ_{N+1} and ϕ_{N+2} is clearly seen on the waveforms.

The output serial register has an output gate which isolates the last phase electrode ϕ_2 from the output diode n* diffusion. Introduction of clock transients on the video may occur because of internal capacitive feedthrough between ϕ_2 and the diode. The clock pulses used to produce







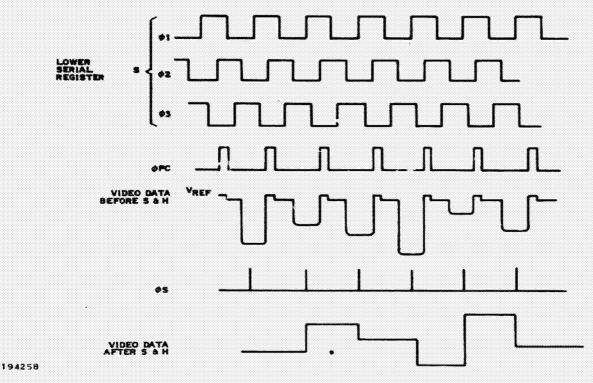


Figure 3-25. Expanded Timing Diagram for Video Output

changes in the potential distribution in the CCD are communicated to the edge of the n⁺ (reverse-biased junction) diode causing current to flow. De bias on the gate allows transfer of minority carriers into the sensor well without a large change in surface potential due to the clock pulse. Possible clock effects on the output video may indicate nonoptimum transfer gate operation.

By changing the bias on the gate it is possible to change the timing of the emergence of the signal charge from the device, as shown in Figure 3-28. The solid lines in the potential profiles of this figure are the potential energy in electron-volts when there is no charge in the channel. The top of the shaded area is the potential profile after the electrons have been introduced. These same figures are applicable to both buried- and surface-channel devices; for a buried-channel device the potentials correspond to the highest voltage in the buried channel, while for a surface-channel device the profiles should be considered to be the surface potential.

In the upper potential profile of Figure 3-28 the output gate is biased at a low voltage (high energy), and the signal charge is collected in the output diode by means of a "charge-pushing" mechanism. Charge pushing occurs when the output gate voltage is greater than the voltage of an off-clock but less than an on-clock voltage. When the last phase (ϕ_2) turns off, the charge will be pushed into the output diode region because of the lower energy barrier (higher voltage) in this direction rather than back into the previous well (ϕ_1) . A noticeable drop in transfer efficiency is found if the output gate is at too low a voltage for the charge pushing to work effectively. If the output gate is biased to a value equal to or greater than the clock voltage, then the signal charge will "spill" out when the last phase (ϕ_2) turns on and as the preceding well (ϕ_1) turns off. At

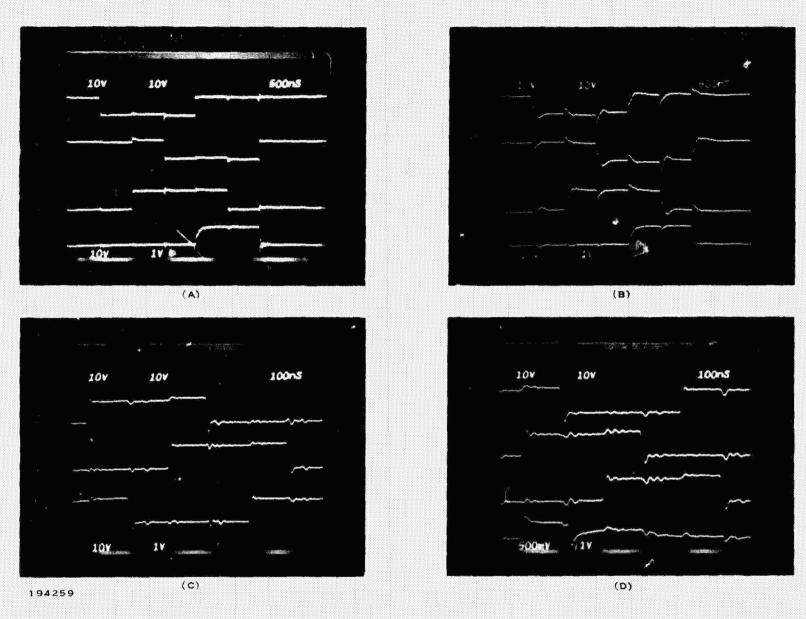
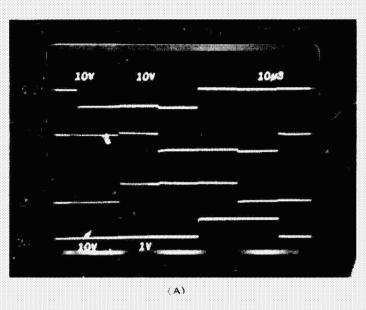
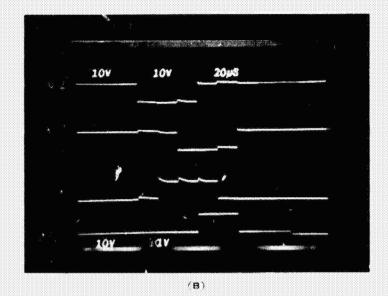
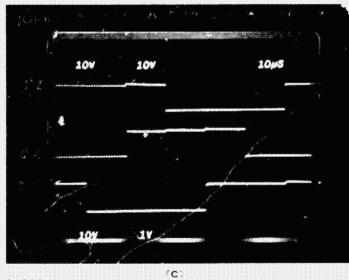


Figure 3-26. Parallel Clock Waveforms Delivered to a Resistive Load (A); To a 400 X 400 CCD (B); Serial Clocks (C and D) 1-MHz Serial Data Rates

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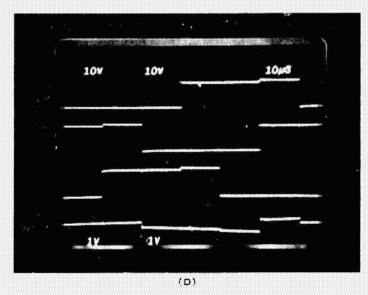
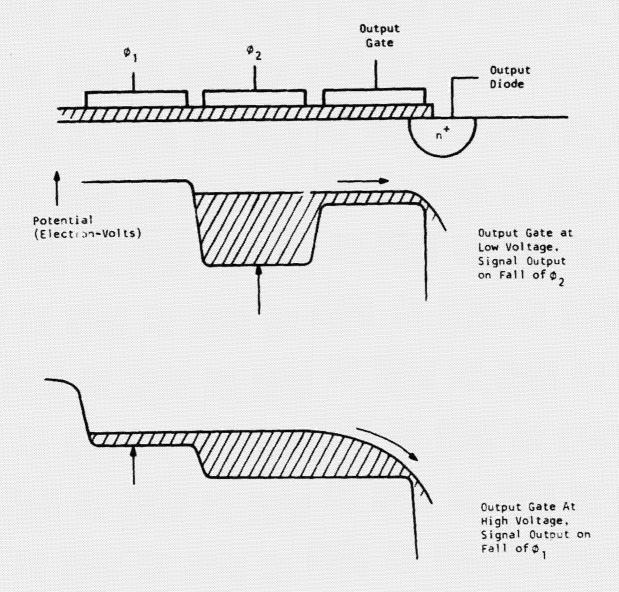


Figure 3-27, Parallel Clock Waveforms Delivered to a Resistive Load (A); To a 400 X 400 CCD (B); Serial Clocks (C and D) 10-kHz Serial Data Rates





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Figure 3-28. Potential Profiles that Demonstrate Effect of Output Gate on Video Output

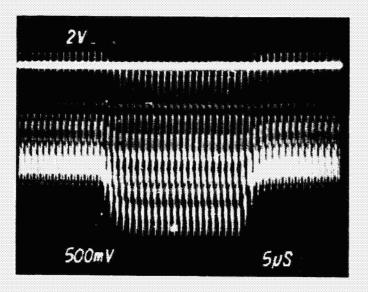


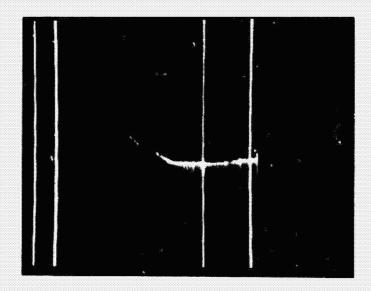
intermediate values of output gate bias the charge can come out at the rise and fall of ϕ_2 as well as at the fall of ϕ_1 , as shown in the lower profile of Figure 3-28.

I. MULTIPROBE OPERATION OF CCDs

After the arrays have been processed prior to imaging evaluation and are still in slice form, they are tested for gate oxide pinholes and metal shorts by a high-speed multiprobe. This test is simply a dc test allows sorting into good and partial 400 X 400's or good and bad 160 X 100's. Much more information can be obtained by operating the devices as CCDs while still in slice form. This is done by supplying to the multiprobe all pulses necessary to operate the imager. Thus, it can be determined if the array will shift charge, its C1E can be measured, and a dark-current signature can be displayed on a monitor. It is not possible to image on the multiprobe at present but the CTE and dark-current tests are very informative. The best bars are then identified, scribed and cleaved from the slice and thinned using the individual chip thinning technique described below. The use of the probe can increase through-put considerably and allow attention to be focused on a good class imager immediately. An example of the results obtained in multiprobe are given in Figure 3-29. This particular 400 X 400 was chosen as it shows a scratch which appeared on the bar somewhere in processing and now appears as a white dark-current generator. This supports the model discussed above where damage (the scratch) results in dark-current spikes. Also shown is CTE data, which is rather noisy due to the long cables to the probe but is sufficient to determine the value for the array. In addition, the sharpness of the defects is a good indication of CTE for the array.







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Figure 3-29. Dark-Current Signature from a 400 X 400 Array on the Multiprobe Operating at 1 MHz with CTF Measurement Shown



SECTION IV BURIED-CHANNEL OPERATION AND DESIGN

This section is intended as a brief introduction to allow the reader some insight into design and operation of buried-channel CCDs.

A. OPERATING VOLTAGES FOR BURIED CHANNEL

In Figure 4-1 a very simple, two-stage n-channel buried channel register is shown. The n-type buried channel layer which has been introduced into the p-substrate has n^+ contacts at both ends. These contacts are referred to as the input and output "diodes." Adjacent to these diodes are input and output gates which are separate from the clock electrodes (ϕ_1 , ϕ_2 and ϕ_3). In this section the considerations involved in determining the voltages required to obtain buried-channel operation with this device are discussed. A simple design technique is given which models the buried-channel layer as an effective threshold shift. The usefulness of the effective threshold for other on-chip integrated circuits which have buried channel MOSFETs is shown by an analysis of the voltages required for a standard precharge output amplifier.

Correct buried-channel operation requires an ion implantation (normally phosphorus) to convert the p-type substrate. In the initial phase of the present program, lack of close control of implant dose and silicon resistivity (acceptor concentration) resulted in very shallow or essentially no buried channel. Such devices are always characterized by lower CTE than would have been the case if no implant at all had been performed. This suggests some surface damage remains, even after annealing.

The implant can be gauged readily by measuring the turnoff voltage for the on-chip MOSFET which, of course, has a buried channel between source and drain. In this program the optimum V_T (as discussed below) for satisfactory, high CTE buried-channel operation was 10 to 12 volts.

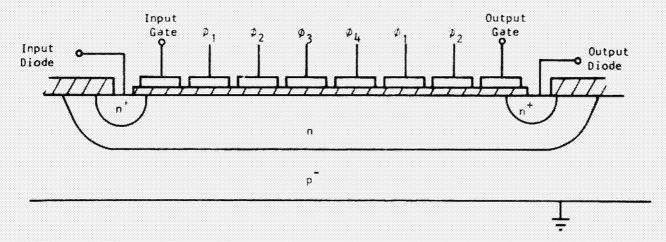


Figure 4-1. Simple Three-Phase Shift Register Showing the n Buried Layer in a p Substrate



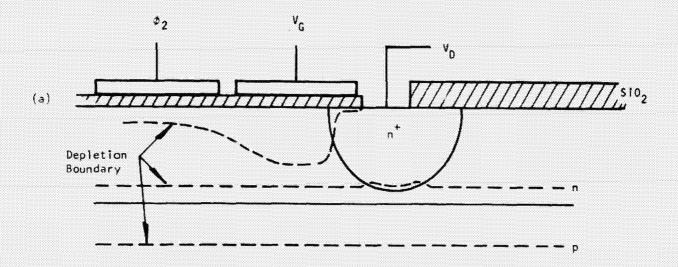
Output Diode and Gate

The constraint on the voltage applied to the output diode is that it be sufficiently 'arge to deplete the buried-channel layer of electrons. Before this depletion occurs, application of a positive clock voltage merely causes accumulation under the clock electrode layer and therefore essentially no modulation of the channel potential occurs. However, after depletion the only electrons that remain in the buried-channel layer are the signal charge (and any leakage), so that the clock electrodes can strongly modulate the potential in the channel. Also, the net positive charge resulting from the bare donor atoms results in potential distribution which moves these electrons away from the surface into the buried-channel layer.

In order to perform this depletion, a positive voltage, V_D, is applied to the n⁺ output diode that serves as a contact to the buried channel n-type layer and reverse-biases this n-region with respect to the p-substrate. If another voltage, V_G, is applied to the output gate, which is negative relative to the n-layer, $V_{\rm G} < V_{\rm D}$, a surface depletion region will extend downward from this gate. If the surface and junction depletion regions do not merge (as in A, Figure 4-2), depletion of the n-layer will not be obtained. The channel potential under the clock electrodes will then be only weakly modulated by the clock voltages that are applied to these gates, because the majority carrier electrons in the n-layer will be accumulated and thus shield the channel from the changing gate potentials. If, however, $V_{\rm p}$ and $V_{\rm D}-V_{\rm G}$ are sufficiently large so that the depletion regions meet, as in B, Figure 4-2, the n-layer under the output gate will be devoid of carriers. If the voltage on the last clock phase (ϕ_2 in Figure 4-1) in the off state is sufficiently below $V_{\rm p}$, the depletion obtained under the output gate will be extended under ϕ_3 . When a positive clock pulse (usually 5 to 15 volts) is applied to this phase (the on-state) a buried channel forms under this gate. This buried channel will act as a sink for the electrons in the next adjacent phase (ϕ_2) , which is off at this time. When ϕ_3 goes off again, the depletion will be re-established under ϕ_3 and the charge from under the ϕ_2 electrode will be swept out the output diode. In this way the depletion will propagate along the channel until the entire n-layer is depleted. As long as the clocking speed is sufficient to prevent the n-region from being resupplied with carriers by leakage currents, the channel will remain depleted. For the area array this process continues through the parallel section until the whole CCD is depleted.

In a design of the buried channel layer, it is important that the voltage required at the output diode for depletion does not exceed any breakdown levels. In order to keep the output diode voltage at as low a level as possible, it is desirable to set the output gate at a low level. A plot of the voltage required for depletion as a function of the output gate voltage is shown in Figure 4-3. These data were taken on a serial register with an average doping concentration of 1 \times 10¹⁶ cm⁻³ for the buried-channel layer and a substrate doping (p-type) of 8 \times 10¹⁴ cm⁻³. For these doping conditions the n-p junction is essentially one-sided under the output gate and the junction depletion region will not extend very far up into the n-layer. The depletion of the channel, therefore, must be obtained primarily by the surface depletion region extending down from the output gate. This explains the almost linear dependence of the depletion voltage on the output gate voltage, because the width of the surface depletion region is only a function of V_D - V_G. The small deviation from linearity occurs because the n-layer junction depletion region is actually increasing by a small amount; thus, slightly less output diode voltage is required. The depletion voltage does not increase with V_G when V_G is greater than the clock voltage (of 8 volts) because the depletion then takes place under the last clock electrode before it depletes under the output gate (i.e., the output gate becomes simply an extension of the output diode diffusion).





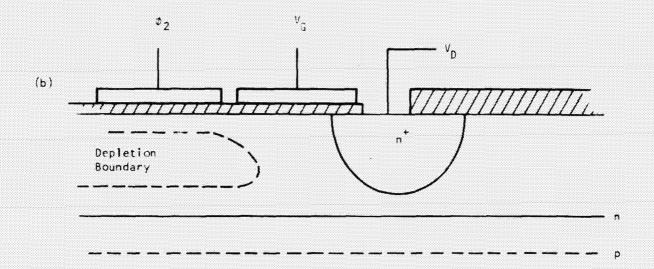


Figure 4-2. Output Circuitry of a BCCCD



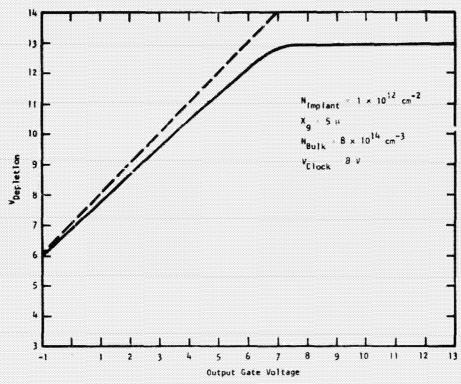


Figure 4-3. Output Diode Voltage for Depletion as a Function of Output Gate Voltage

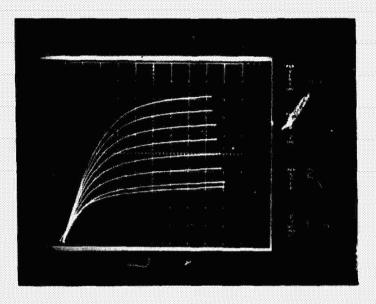
It is useful to consider the effect of the buried channel layer as simply a modification of the threshold under the output gate which, along with the output diode, is essentially half of a MOSFET. The voltage required on the output diode for depletion, V_{DEPL} , is then simply given by

$$V_{DFPL} = \alpha V_{G} - V_{FFF}$$
 (4-1)

where V_{EFF} is the effective threshold resulting from the buried-channel layer. Typical values for this threshold range from -5 to -15 volts. The factor α represents the degree of modulation of the channel potential by the applied gate potential. For shallow buried channels this factor is nearly 1 and decreases for deeper channels. Calculations of α and V_{EFF} are made below.

The reason that the threshold shift due to the buried channel is termed an effective threshold can be seen from the transistor characteristics shown in A. Figure 4-4. An attempt to apply the usual definition of threshold to such a device fails because the drain current, I_D , cannot be cut off by decreasing the gate voltage. The only way in which this transistor can be cut off (which is equivalent to depletion of the buried channel) is to raise the potential (relative to the substrate) of the source diffusion (the drain voltage is always greater than the source) so that the gate bias is at least an effective threshold below the source. The curves in B, Figure 4-4, are shown with $V_{SOURCE} = \pm 15$ V and a V_{TI} for this device is about 12 volts. It can be seen from this figure that when the gate is 12 volts relative to the source, the buried-channel layer has been depleted and the drain current can be cut off.





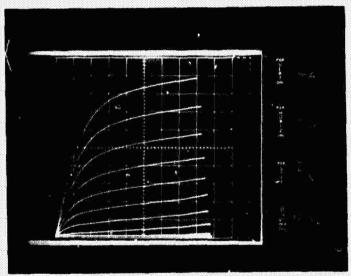


Figure 4-4. In Versus VD for Buried-Channel MOSFET With Substrate Voltage of 0 Volt and 15 Volts

Another example of the usefulness of the effective threshold is determination of operating voltages to be expected from a simple precharge output circuit (reset switch and source follower) shown earlier as the initial part of the BSHA amplifier. The source-follower transistor should be made buried channel to reduce the 1/i noise contributions because the signal charge does not interact with surface states. The precharge transistor should be a buried-channel device because lower voltages are required at the $\phi_{\rm RC}$ gate to precharge the node to $V_{\rm REF}$.

The constraint on the voltage V_{RFF} is that it be large enough to satisfy

$$V_{REF} \ge \alpha V_{OG} - V_{i+1}$$
 (4-2)



in order to bias the output diode at a sufficiently high voltage to ensure depletion of the CCD buried channel. Bias on the source-follower should be set so that there is low current flow through the device in order to eliminate interaction of the signal current with the surface states (and thereby obtain increased 1/f noise). In this condition this transistor is nearly cut off and the source (output) will then be at a voltage.

$$V_{S} = \alpha V_{RFF} - V_{EFF}$$
 (4-3)

In order to bias this device in the saturation region the drain should be at a voltage given by

$$V_{\rm D} > \alpha V_{\rm RH} - V_{\rm EFF} \tag{4.4}$$

Therefore, all bias voltages needed for this buried-channel output can be determined once the effective threshold of the buried channel layer has been obtained. In Subsection III.B calculations are made of $V_{\rm EFF}$ for a variety of buried channel layer dopings and distributions. $V_{\rm EFF}$ is typically about 11 volts for buried-channel CCDs, implying ~30 V for $V_{\rm D}$. If the source-follower is not buried channel, $V_{\rm EFF}$ ~0 volt and $V_{\rm d}$ need only be ~18 to 20 volts.

2. Electrical Input of Signals

Usefulness of the effective threshold extends to the input circuitry as well. If the input ω introduced through the input diode and the clock voltage, V_C , is applied to the input gate (either pulsed or dc), the voltage required on the input diode V_{ID} to keep from introducing signal must satisfy

$$V_{1D}$$
 (empty well) $\geq \alpha V_C - V_{EFE}$ (4-5)

If the clocks are pulsed from 0 to V_C, the voltage level for a full well is given by

$$V_{1D}$$
 (full well) $\approx V_{1EF}$ (4-6)

where α depends on the distribution of the buried-channel layer but typically ranges from 0.7 to 0.9.

In the low-noise charge extraction input technique, the input diode is pulsed and the signal introduced on the input gate. The diode must then be pulsed between the levels given in Equations (4-5) and (4-6).

The usefulness of the effective threshold in design is again obvious and in Subsection III.B the method of calculating this voltage level is discussed.

B. CALCULATION OF EFFECTIVE THRESHOLD

in order to calculate the effective threshold it is only necessary to calculate the onedimensional potential profile in the direction perpendicular to the silicon surface. It is possible to obtain analytic expressions for this profile without charge if a sufficiently idealized doping distribution is assumed for the buried-channel layer. One very useful such doping distribution is the box distribution, which is a close approximation to the profile obtained in epitaxial material. Another technique for introducing the buried-channel layer is to use an ion implantation with a



drive n diffusion. The profile obtained with this technique is Gaussian, and calculation of the potentials with this distribution require numerical techniques. The effective threshold will be calculated for the box distribution in some detail and then results will be given for more complex distributions.

1. Box Distribution

For an n-channel device the box distribution assumes a constant doping density of N_D of width X_J beneath the oxide and a density of N_A in the p-region as shown in A, Figure 4-5. If the assumption is made that the n-region has been completely depleted of electrons and if the depletion width is of length X_W in the p-material, the charge distribution which results is shown in B, Figure 4-5. The potential has a useful form at the p-n junction boundary, $X = X_J$, where previous calculations have shown it to be given by

$$\phi(X_1) = [(V_G - V_{FB} + \alpha^2)^{1/2} - \alpha], \qquad (4-7)$$

$$\alpha = \left(\frac{\epsilon_{Si} N_A}{2}\right)^{1/2} \left(\frac{X_{ox}}{\epsilon_{ox}} + \frac{X_J}{\epsilon_{ox}}\right)$$
 (4-8)

$$V_{FB}' = V_{FB} - N_D X_J \left(\frac{X_{ox}}{\epsilon_{ox}} + \frac{X_J}{2\epsilon_{Si}} \right)$$
 (4-9)

$$V_{EB} = \psi_{ms} - \frac{Q_{ss}}{(\epsilon_{ox}/X_{ox})}$$
 (4-10)

and

 $\epsilon_{\rm ox}, \epsilon_{\rm Si}$ = dielectric constant of the oxide and silicon

 ϕ_{ms} = metal-semiconductor work-function difference

Q = fixed positive charge

 X_{ox} = oxide thickness

 V_G = applied gate voltage.

Typical values for V_{FB} are -1 to -2 volts, but for convenience in all numerical results V_{FB} will be set to zero. The effect of V_{FB} is merely to shift the gate voltage by $-V_{FB}$. The distance of the peak voltage in the channel from the oxide-silicon interface, X_{max} , can be calculated from

$$X_{1:tax} = X_j - \left(\frac{N_A}{N_D}\right) - (X_W - x_j). \tag{4-i1}$$



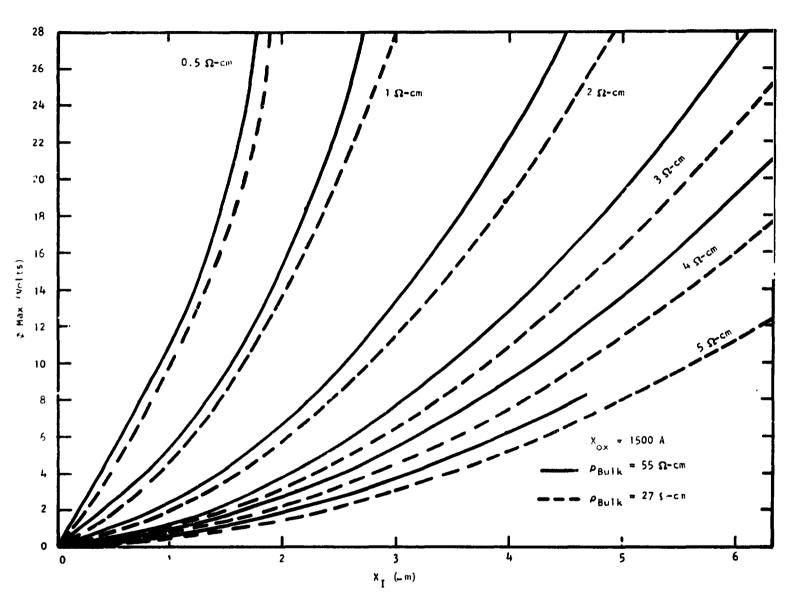


Figure 4-5. Buried-Channel Charge and Potential Profiles for Box Distribution



where X_w is the edge of the depletion width in the p-region and which satisfies the relation,

$$X_{W} = \left[\frac{2\epsilon_{Si}\phi(X_{J})}{qN_{A}}\right]^{\frac{1}{2}} + X_{J}$$
 (4-12)

Using Equation (4-12), the peak voltage in the channel $\phi(X_{max})$ can then be found to be

$$\phi(X_{\text{max}}) = \left(1 + \frac{N_A}{N_D}\right) \phi(X_J)$$
 (4-13)

The lower part of Figure 4-5 summarizes these results.

In order to deplete the buried channel the quasi-Fermi level for the electrons must be raised above ϕ_{\max} . The quasi-Fermi level can be raised by increasing the voltage applied to the output diode, which is really only a contact to the n-type buried-channel layer. The effective threshold is, therefore, the difference between ϕ_{\max} and the gate voltage, i.e.,

$$V_{EFF} = \phi_{max} - V_{G} \tag{4-14}$$

which can be evaluated using Equations (4-7) and (4-13).

In Figure 4-6 the effective threshold at ... It gate bias V_{EFF} is given for substrate resistivities of 13 ohm-cm and 4.5 ohm-cm (which correspond to acceptor concentrations of 1 \times 10^{15} cm⁻³ and 3 \times 10^{15} cm⁻³, respectively). The range of n-layer resistivities, ρ_{epi} , covered is from 0.5 ohm-cm to 5 ohm-cm with thicknesses up to 6 μ m. These curves were obtained assuming an oxide thickness of 1500Å. However, dependence of these curves on oxide thickness is very weak, so that the error in ϕ_{max} for oxides as thin as 1000Å or as thick as 2000Å is less than 1 volt. In the limit of light doping in the bulk and a junction depth large relative to the oxide thickness $X_1 \gg X_{ox}$ the expression for V_{EFF} reduces to:

$$V_{EFF} = V_{FB} - \frac{N_D}{2\epsilon_{S_1}} - X_J^2$$
 (4-15)

where F_{FB} is given in Equation (4-3). In this limit, V_{EFF} is independent of gate voltage and hus the modulation of ϕ_{max} in the buried channel is equal to changes in the applied gate potential, i.e., the channel modulation factor, α , which was defined in Equation (4-1) is unity. As the substrate do ng is increased, α will decrease.

2. Gaussian Doping Distribution

The doping profile (Figure 4-7) for an impurity, $N_D(X)$, which is introduced by a shallow ion implantation followed by a drive-in diffusion into a bulk acceptor density of N_A , yields a doping profile, $\rho(X)$, given by



$$\rho(X) = \frac{2N_{\text{Dose}}}{\sqrt{\pi} X_g} e^{-(X/X_g)^2} - N_\chi$$
 (4-16)

where N_{Dose} is the total dose of the implant and $X_g = 2\sqrt{D}t$, where D is the diffusion coefficient of the impurity and t is the time of the diffusion. It is not possible to obtain an analytic expression for the potentials using this Gaussian doping distribution; instead, iterative techniques must be used.

The one-dimensional potential $\phi(X)$ is obtained by solving Poisson's equation, subject to the appropriate boundary conditions. If the coordinate system introduced in Figure 4-5 is used, the following result for X > 0 is obtained:

$$\phi(X) = V_G - V_{FB} + \left[-N_{Dose} \operatorname{ert} \left(\frac{X_W}{X_g} \right) + N_A X_W \right] \left(\frac{X_{ox}}{\epsilon_{ox}} + \frac{X}{\epsilon_{S1}} \right) + \gamma(X)$$
 (4-17)

where

$$\gamma(X) = \frac{2N_{\text{Dose}}}{\sqrt{\pi}X_{g}\epsilon_{S1}} \int_{0}^{X} dX_{2} \int_{0}^{X_{2}} e^{-(X_{c}/X_{g})^{2}} dX_{1} - \frac{N_{A}X^{2}}{2\epsilon_{S1}}$$
(4-18)

If the integrals are evaluated, then $\gamma(X)$ is given by

$$\gamma(X) = \frac{2N_{\text{Dose}}}{\sqrt{\pi}X_{\text{g}}\epsilon_{\text{S1}}} \left\{ \frac{\sqrt{\pi}}{2} X X_{\text{g}} \operatorname{erf}\begin{pmatrix} X \\ X_{\text{g}} \end{pmatrix} + 0.5 X_{\text{g}}^{2} \left[e^{-(X X_{\text{g}})^{2}} - 1 \right] \right\} \frac{N_{\text{A}}X^{2}}{2\epsilon_{\text{S1}}}$$
(4-19)

where erf(X) is the error function. Using the boundary condition that $\phi(X_W) = 0$, a simple equation can then be written for X_W which must be solved iteratively.

$$X_{W} = \begin{bmatrix} N_{\text{Dose}} & \text{erf} \begin{pmatrix} X_{\text{max}} \\ X_{g} \end{pmatrix} + \begin{pmatrix} \gamma(X_{W}) + V_{G} & V_{EB} \\ \vdots & \vdots & \vdots \\ \zeta_{S1O_{2}} & \zeta_{S_{1}} \end{pmatrix} \end{bmatrix}$$
(4-20)

Once X_W is obtained, the potential at any point in the channel can be obtained by use of Equation (3-17). The surface potential $\phi(0)$ is therefore given by

$$\phi(0) = V_G - V_{FB} - N_{Dose} \operatorname{erf}\left(\frac{X_W}{X_g}\right) + N_A X_W$$
 (4-21)

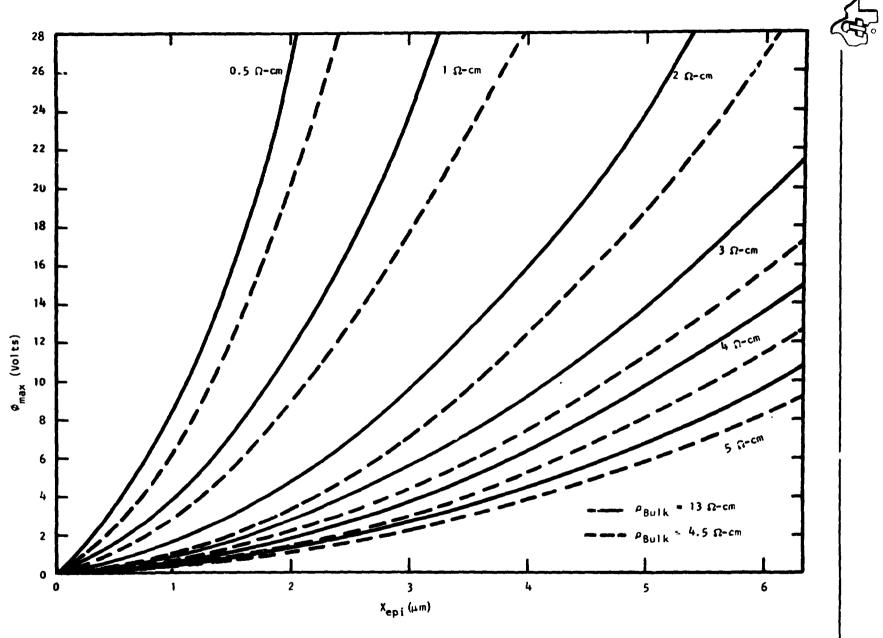


Figure 4-6. Maximum Potential in the Channel for a Box Distribution



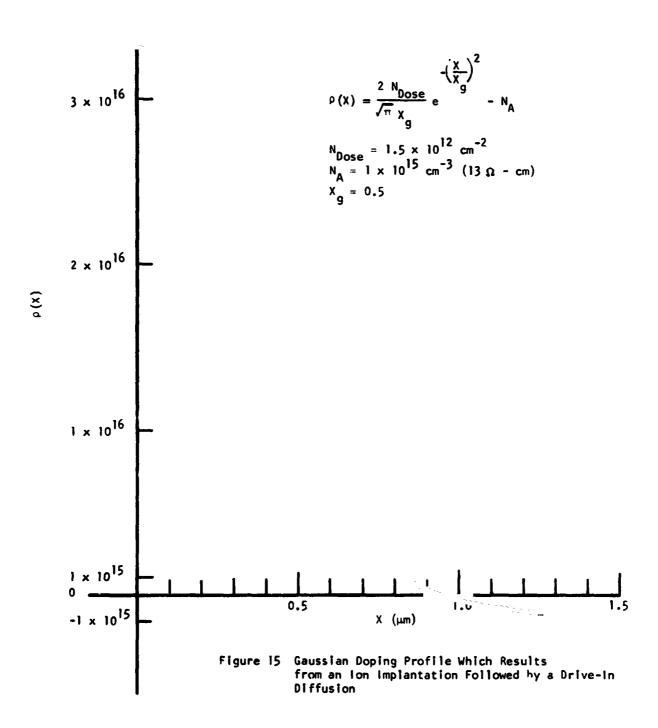


Figure 4-7. Gaussian Doping Profile Resulting from an Ion Implantation Followed by a Drive in Diffusion

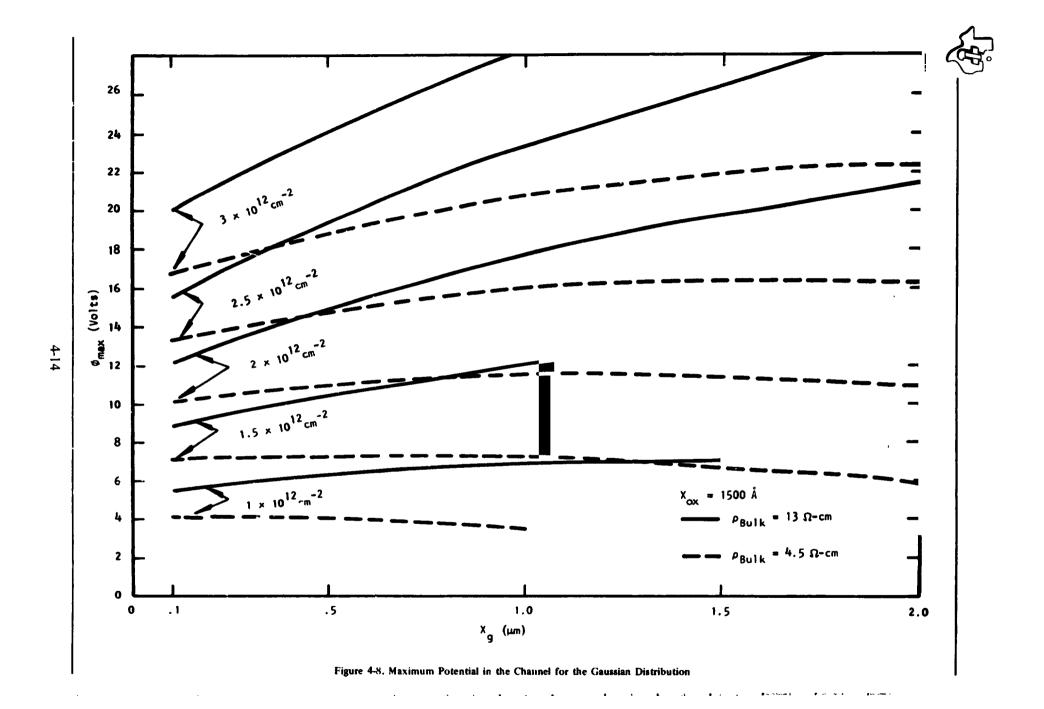


To obtain the maximum potential in the channel, ϕ_{max} , and the depth of that point, X_{max} (Figure 4-5) the derivative of Equation (4-17) is taken and set to zero. The condition for X_{max} is shown in the low. part of Figure 4-5, i.e.:

$$V_{EFF} = \phi_{max} - V_{G}$$

A plot of $V_{\rm EFF}$ for substrate resistivities of 13 ohm-cm and 4.5 ohm-cm is given in Figure 4-8 as a function of a depth of the implant $X_{\rm G}$.

An important point to note is that the dependence of the effective threshold on implant depth is relatively weak and since it is possible to control the implant levels accurately, close control on effective threshold can be maintained.





SECTION V DEVICE TESTING AND CHARACTERIZATION

A. CCD ENVIRONMENTAL CAMERA

The CCD is placed in a special environmental camera and cooled to -40° C by nitrogen gas which has passed through an external copper coil immersed in LN₂. The camera also has capability of operating at any desired temperature from -60° to $+60^{\circ}$ C. Temperature is measured by a platinum resistance coil (located directly behind the CCD) and digital thermometer. A ring-shaped entrance and exit nozzle for the cooling gas ensures uniform temperatures inside the camera and, because the cooling gas is in direct contact with the CCD membrane, self-heating and temperature graJients across the membrane can be ignored. Thus, it is expected that the CCD membrane and platinum coil are at the same temperature. This was tested by connecting a constant current source to the serial input diode of the CCD and measuring the forward voltage drop of the diode as a function of temperature. The temperature ratio calculated from the ratio of forward voltage drops gave a CCD membrane temperature within 1° C of -40° C when the digital thermometer read -40° C.

The temperature is maintained at -40° C by a second platinum resistance coil located behind the CCD and connected to a proportional controller which drives an electro-pneumatic converter. The converter changes the pressure and hence the gas flow through a heat exchanger coil and thus actively maintains the correct temperature.

The camera is an evacuated, double-wall stainless steel design with double optical windows on a removable faceplate. The CCD header and connector are mounted on a gimbal inside the camera. Mechanical feedthroughs passing through the vacuum wall permit ± 3 degrees rotation of the CCD header about two orthogonal axes and ± 3 nm of translation in two directions at right angles with respect to the camera axis of rotation. The lens is a Wollensak 65 mm f/4.5, Micro Raptar lens mounted on a focusing cell which is concentric with the windows and the axis of rotation of the camera.

Since the entire camera is mounted on a 360-degree rotator, it is possible to image with the CCD and adjust the internal gimbal so that the imaged scene appears on the monitor to rotate about the center pixel of the CCD, while at the same time the four corners of the array are in focus. This guarantees that the CCD is aligned with the geometric axis of the lens, a consideration of importance when making lens corrections to the square-wave amplitude response. The experimental apparatus showing the Dewar and electronics developed for this program are shown in Figure 5-1.

B. MULTICHANNFL ANALYZER TECHNIQUES

A multichannel analyzer (MCA) interfaced with a calculator is used in one technique for measuring dark current as well as in measurements of noise and uniformity of response. The MCA is operated in the sample voltage analysis (SVA) mode, where the voltage at the input of the MCA is sampled at a time determined by an externally derived strobe pulse, and the channel corresponding to the sampled voltage has its contents incremented by one count. If each pixel amplitude is sampled as it is read out of the CCD, the result of the SVA mode is to give a plot





Figure 5-1. CCD Evaluation Apparatus Showing Low-Temperature Gas Flow Dewar (Sheet 1 of 2)



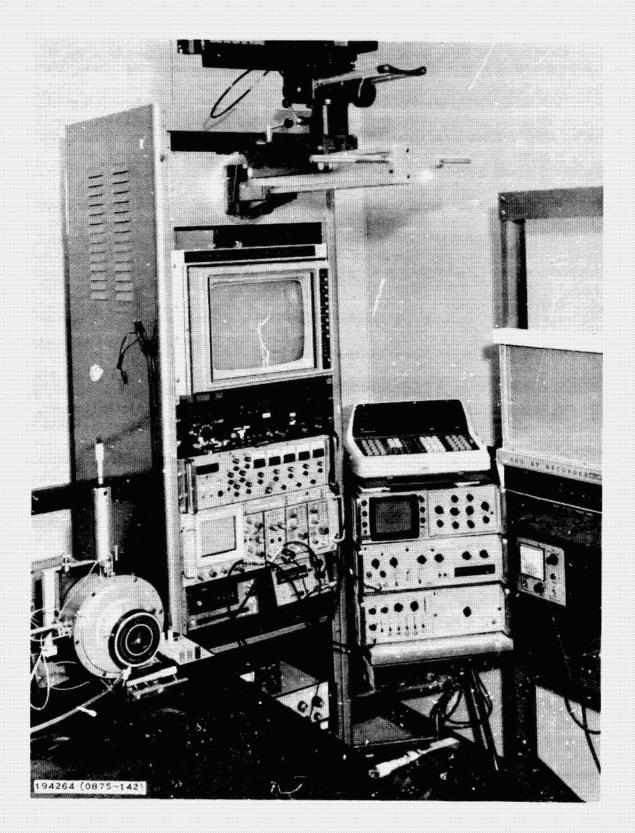


Figure 5-1. CCD Evaluation Apparatus Showing Low-Temperature Gas Flow Dewar (Sheet 2 of 2)



of the number of pixels having a given voltage amplitude versus the voltage amplitude. This plot can be displayed on a CRT and photographed. In addition, an HP 9820 calculator, which is interfaced with the MCA, can sample the contents of the 1024-channel memory of the MCA and perform arithmetic operations on the contents, such as finding averages and standard deviations.

The MCA is a Hewlett-Packard 5401B interfaced with a Hewlett-Packard 9820A calculator. There are 1024 channels of memory with 10^6 counts per channel and a conversion gain ranging from 4096 channels/10 volts to 512 channels/10 volts. System dead time after each voltage sample ranges from 31.5 to 7.5 μ s, depending on the conversion gain. It is impossible to sample successive pixels spaced closer than the dead time. At a 10 kHz data rate each pixel can be sampled successively, but at 1 MHz, for a conversion gain of 1024 channels/10 volts, the dead time is 10.5 μ s, corresponding to 10.5 bits. In this case the strobe pulse must not be generated at the data rate but rather, for example, every 15 bits. This pattern of every 15 bits is incremented in phase by 1 bit once each frame, so that after 15 frames every pixel has been sampled. This pattern sampling can be accomplished by a so-called bar-dot generator, which also has the capability of providing rasters that are phase locked.

C. DARK CURRENT

At room temperature, dark current can be realiably measured by either an integration technique or by precharge current measurements.

The precharge current methor is accomplished by measuring the precharge current I_{pc} (1) of the CCD under normal operating conditions and subtracting the precharge current I_{pc} (2), measured with the serial register operating in reverse so that array dark current is shifted to the input diode. $I_{pc}(2)$ is amplifier and header leakage. For the 160×100 array, reverse operation of the parallel section is possible with dark current being removed via the upper serial register. The dark-current contribution of the serial register only can therefore be determined. For the line scanners, the 10 lines and serial register are assumed to generate equal dark currents per unit area. The dark-current density is

$$J_D(PC) = I_D(PC)/A$$

where A is the active array area

$$A = Nd_x d_v + d_x' d_v'$$

N = Number of pixels, d_x , d_y pixel dimensions in parallel section d'_x , d'_y pixel dimensions in serial register (0.9 × 1.0 mil²).

The integration technique of dark-current measurement begins with a current-to-voltage calibration of the output amplifier and external circuitry to the MCA. This is done by injecting current I(V) at the input to the serial register and measuring the video voltage with the MCA with the serial register operating at a frame time τ_F . This is done for several values of input current and a calibration factor, K_1 volts/ampere, is obtained from a plot of I(V) versus V. During this measurement the parallel clocks are turned off to minimize dark current from the array. However, input current can be easily made much higher than this dark current contribution, so the value of K_1 is accurately determined.



The array is returned to normal operation and an integration time chosen to allow accumulation of dark carriers amounting to 5 to 15 percent of a full well. This population level ensures that the resulting video voltage is above drift in the amplifier chain prior to the MCA. After the required integration time, the device is read out to generate V_v volts. A plot is made of V_v against frame time, τ_F , to obtain a factor K_2 volts/second, which can be simply related to the dark generation of carriers. The dark-current generation rate is essentially independent of well population up to at least 15 percent full well, allowing a unique value of K_2 to be determined. The dark current is simply

$$I_D = K_2 \tau_E / K_1$$
 ampere

Although the integration method is more tedious than the precharge method of measuring dark currents, the integration technique must be used at low temperatures where header and amplifier leakage currents may be much higher than the dark current being measured. At room temperature, where header and amplifier leakages are generally much smaller than the dark current, good agreement has been found between the two methods.

D. DARK CURRENT UNIFORMITY AND BLEMISHES

With the CCD in complete darkness and after an integration time sufficient to produce a dark video voltage signal well above the drift in the amplifier chain to the MCA, the device is read out and the distribution accumulated in the MCA. The dark nonuniformity is defined as the RMS deviation of the distribution divided by the mean. Dark-current blemishes, defined as the number of pixels contributing signals ≥ 4 percent of full well are counted by the MCA. Blemishes defined in this way do not distinguish between localized dark-current spikes and high regions of generation, for example at the corners of the array due to heating effects of on-chip amplifiers.

E. SPECTRAL RESPONSE

The responsivity, K, can be measured in the following manner. The imager is uniformly illuminated, and the precharge current, I, is measured as a function of incident photon power, P. Under the assumption

$$I = K P^{\gamma} + I_{D}$$

a plot of $\ln (I - I_D)$ versus $\ln P$ should result in a straight line of $\operatorname{slop} \gamma$. (K is called the responsivity and I_D is the dark current, including all leakage contributions.)

For current levels below nominal saturation it is expected that γ is a constant having a value $\cong 1.0$. The constant K is termed wideband responsivity (K) or spectral responsivity (K_{λ}), depending on whether the light source is wideband, or narrowband centered about λ . The responsivities obtained at a given well population (i.e., given $I - I_D$ and frame time τ_F) by the prescription ($I - I_D$)/P are defined as wideband sensitivity (S) or spectral sensitivity (S_{λ}).

It should be pointed out that if γ is not unity, then $S = (I - I_D)/P$ depends on P. If K is measured in units of amperes/watt⁷, then if γ is slightly different from unity, K can be significantly different from S at the 1- μ W level. For example, suppose $\gamma = 0.95$ and K = 0.100 ampere/watt^{0.95}. At the 1v ** level S = 0.100 × (1.00)^{0.95}/1.00 = 0.100 ampere/watt, but at the 1- μ W level, S = 0.100 × $(10^{-6})^{0.95}/10^{-6} = 0.200$ ampere/watt. Thus, to make K more



representative of S at the incident power levels of interest, the units of K are chosen as nanoamperes/microwatt^{γ}. In this case, at the 1- μ W level, S and K are identical. However, $\gamma \neq 1$ should be regarded as an experimental problem. Recent data on many arrays at Texas Instruments shows $\gamma = 1$ within better than 1 percent for a large number of arrays tested.

Once K_{λ} has been obtained at each wavelength, it can be plotted as a function of λ . However, to avoid this tedious but of data taking, we plot, instead, spectral sensitivity, S_{λ} , measured at a fixed well population, i.e., fixed precharge current level, where

$$S_{\lambda} \equiv (I - I_{D})/P_{\lambda}$$

The quantum efficiency (QE) of the device is defined as the number of charge carriers accumulated in the depletion wells per incident photon, at a given photon wavelength. From this definition we have

QE = (hc/e)
$$S_{\lambda}/\lambda = 1.24 S_{\lambda}/\lambda$$

where S_{λ} is in amperes/watt and λ is in micrometers.

For purposes of rapid comparison, the spectral sensitivity of the imager is plotted together with curves of constant quantum efficiency. Note that from the above definition of QE, reflection losses lower the QE, and these losses are not corrected for in the data that are presented.

The experimental setup for spectral sensitivity is the following. A 3400°K source is provided by a tungsten halogen lamp. The light beam passes through a set of neutral-density filters which are mounted in slides at 45 degrees to the beam in a light-tight box. Light reflected from the filters is trapped by a parallel array of thin, blackened plates. This prevents light from bypassing the filters and makes the filters additive to a good approximation. The filters have densities of 0.1, 0.3, 0.5, 1, 2, 3, and 4, so that light can be attenuated up to a factor of $10^{10.9}$, ignoring light leakage and multiple reflections. A spectral filter wheel is interposed between the neutral density filter box and the environmental camera. The spectral filters are thin-film interference filters. The lens is removed from the camera for all nonimaging tests.

The light level is varied by the neutral density filters to keep the CCD well population roughly the same for each wavelength selected by the filter wheel. The total filter density that is recorded for each wavelength, and the CCD precharge current is measured by a Keithley 616A autoranging digital picoammeter. The integration time must be reduced to a near zero value in all tests involving precharge current measurements so that the device is continuously clocking out charge into the picoammeter. Otherwise, the picoammeter does not provide an accurate time-average current measurement. When these measurements are complete the CCD is removed from the light beam and a silicon detector probe is placed in exactly the same position for light intensity measurements. A Tektronix J16 radiometer and J6502 silicon detector probe are currently being used.



The wideband sensitivity, S, can be computed from the measured spectral sensitivity, S_{λ} , numerical integration of the relation

$$\left[\int_{0}^{\infty} S_{\lambda} (dP_{\lambda}/d\lambda) d\lambda\right] / \int_{0}^{\infty} (dP_{\lambda}/d\lambda) d\lambda \equiv S \text{ (itg)}$$

where $dP_{\lambda}/d\lambda$ is the blackbody spectral power distribution for the source temperature, T, desired:

$$dP_{\lambda}/d\lambda \propto \lambda^{-5} \left[\exp(hc/\lambda kT) - 1 \right]^{-1}$$

F. SATURATION LEVEL

Various definitions of saturation level in a CCD have been proposed by different workers. One relatively common definition is based on the measurement of wideband signal transfer of the imager. In this measurement, the imager is uniformly illuminated with a wideband light source and precharge current, I, is measured as a function of incident photon power, P. If $I - I_D$ is then plotted on log-log paper, the resulting curve will be a straight line over a certain part of the range, with slope approximately unity. If the relation

$$I = K P^{\gamma} + I_D$$

is assumed, the slope on log-log paper is γ . Thus, γ is constant and approximately unity over part of the range. For higher values of P, γ will begin to decrease as the CCD becomes so saturated with charge that carrier recombination (or removal at some point other than the precharge terminal) increases faster than carrier photogeneration. Saturation level is then defined as the power, charge, or current level at which γ reaches some arbitrarily selected value, for example, 0.8.

The definition of saturation should reflect the upper limit of the useful operating range of a sensor. The definition in terms of γ does not always meet this criterion. For example, in many CCD imagers, blooming of charge from one pixel to the next will occur before γ begins to decrease appreciably. In such a case, saturation should be defined as the level at which the onset of blooming occurs. Unless certain special design and operational steps are taken to control blooming, the useful range of virtually all CCDs will be limited by blooming rather than by γ decrease. For this reason, the maximum well population at the onset of blooming has been adopted as the definition of saturation level for the measurements made under this program.

The procedure by wl ich this level is determined is as follows. A Nyquist frequency horizontal bar pattern (bars parallel to the output serial register) is focused on the device, and the resulting video is observed on an oscilloscope. The intensity of the light is increased until the output level of illuminated pixels suddenly stops increasing, and the output level of unilluminated pixels begins to increase. At that point, the output voltage corresponding to the peak of the bright bars is measured on an oscilloscope. From this voltage is subtracted the output voltage obtained in



the absence of an optical input. The resulting signal voltage, V_{SIG} , is then converted to the equivalent well population.

G. NOISE AND DYNAMIC RANGE

Measurements of temporal noise were made using the on-chip BSHA circuit with the internal sample gate biased on so that the output is essentially a simple precharge amplifier output. The dummy output is not used. The signal output is fed into an off-chip double sampling circuit, similar in function to the on-chip CCA circuit described in Section II.B of this report. This circuit removes noise resulting from presetting the output node, which would be the dominant temporal noise source on these devices. Only one pixel is sampled per frame, so that fixed pattern (spatial) noise sources will not affect the measurement. The rms noise level on this single pixel is determined by amplifying the noise level with a low-noise preamplifier (gain = 100) and after further amplification, storing this level in a multichannel analyzer. After repeated samples have accumulated in the MCA, the variation of this level is analyzed using the HP 9820 calculator to determine the standard deviation of the resulting Gaussian amplitude distribution. Usually, the video channel is low-pass filtered prior to the double-sampling circuit, to a bandwidth of about twice the clock frequency, or about four times the Nyquist frequency. This reduces the amount of wideband amplifier noise aliased into the measurement by the sampling circuit, which is not an intrinsic noise source in the CCD. The resulting rms voltage determined from the MCA data is then converted to an equivalent rms number of noise electrons per charge packet using the total measured video gain, and the relation between signal voltage (at the CCD output node) and well population.

Operation of a clamp-sample-and-hold circuit (CSH) is shown schematically in Figure 5-2. The circuit is composed of three MOSFET switches, S_1 , S_2 , and S_3 ; three buffer amplifiers, A_1 , A_2 , and A_3 ; and two intentionally introduced capacitors, C_C and C_{SH} . Also shown in the figure is a low-pass filter following amplifier A_1 , which, for simplicity in analysis, is a simple single-pole, low-pass filter characterized by R_1 , C_1 .

Operation of the circuit begins at time t_o by the switch S_1 closing (Figure 5-3 shows a typical waveform) and charging the stray capacitance C_o to the voltage level V_{ref} . The "on" channel resistance of switch S_1 introduces a thermal noise voltage component on the final value of voltage attained at node 1. The equivalent number of noise electrons resulting from this operation is $(kTC_o)^{\frac{1}{2}}q^{-1}$. In terms of the waveforms shown in Figure 5-3, this is manifested as an instantaneous uncertainty in the voltage of the waveform from time t_1 to t_3 , which is given by $(kT/C_o)^{\frac{1}{2}}$. This uncertainty which appears at nodes 2 and 3 of Figure 5-2 is eliminated by closure of switch S_2 at time t_2 . This sets node 3 to a known reference, V_{clamp} . The uncertainty in initial preset voltage at node 1 is stored on C_C and is, therefore, effectively removed from node 3. Signal charge is then sensed as a shift in the voltage at time t_3 . For further signal-to-noise improvement, the signal level is sampled and held at node 4 at time t_4 .

Dynamic range is defined as the ratio of saturation well population to rms number of noise electrons.



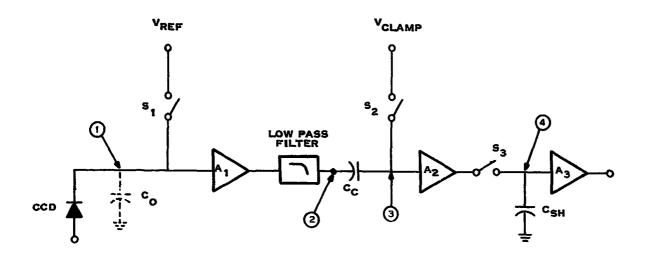


Figure 5-2. Schematic of Basic Clamp Sample-and-Hold Circuit

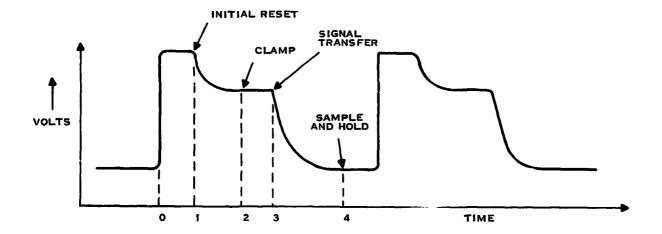


Figure 5-3. Waveform Observed at Nodes 1, 2, and 3 of Figure 5-2



H. RESPONSE NONUNIFORMITY AND BLEMISHES

The uniformity of response of the CCD to incident light is determined by sampling the video with the MCA. Care is necessary to avoid saturating parts of the CCD at high light levels. Again, the mean and the standard deviation are calculated from the video. The response nonuniformity is defined as the ratio of the standard deviation to the mean. The mean video level is recorded, expressed as a percentage of saturation level. This measurement is made for two different illumination cases: wideband (usually 3400° K color temperature) and narrowband, at a wavelength of $0.4 \, \mu m$. In addition to the MCA measurement, photographs are also taken of the monitor display and of oscilloscope traces of a single line and a full frame of the video waveform.

The blemish count is made by a calculator program which determines the number of pixels contributing signals from 0 to 0.75 V_{mean} and above 1.25 V_{mean} . The blemish count does not distinguish between gradual changes in responsivity across the device which can occur due to nonuniform membrane thinning and the isolated blemished pixel.

I. CHARGE-TRANSFER EFFICIENCY

Charge-transfer efficiency (CTE) measurements for the serial register are made by electrical input of a square pulse at the serial input diode. To facilitate CTE measurements as a function of bias charge level (fat zero, FZ), a square pulse of amplitude E_o is offset by an amount E_{FZ} (B, Figure 5-4).

The resulting video output is shown schematically in Figure 5-4. The reference level for zero FZ ($v_{FZ}=0$) is determined by increasing E_{FZ} at the input diode until the video output level remains stationary for further increases in E_{FZ} . The saturation level V_{SAT} or full-well condition for this measurement is determined by decreasing E_{FZ} until the video output level remains stationary for further decreases in E_{FZ} , or until the output pulse train begins to spread due to blooming, whichever occurs first. The amounts of fat zero and video signal are expressed as fractions given by v_{FZ}/v_{SAT} and $v_{T}/(v_{SAT}-v_{FZ})$.

It can be shown that the charge transfer efficiency is given by

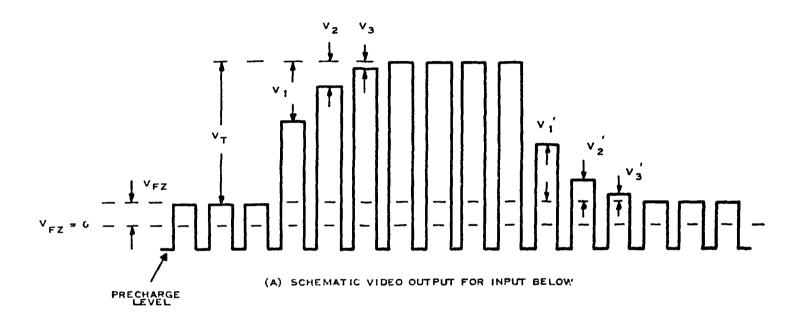
CTE =
$$1 - \epsilon$$

where ϵ is the transfer inefficiency given by

$$\epsilon = \left(\frac{1}{Nv_1}\right) \sum_{i} v_i$$

N = number of transfers, v_T is the steady-state signal voltage, and v_1 (i = 1, 2, 3, ...) is the voltage decrement in the *ith* pulse of the output signal packet, as shown in Figure 5-4. For the 100 X 160, N = 3 ×160 = 480.





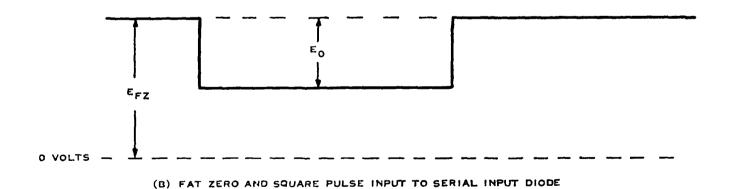


Figure 5-4. Fat Zero and Square-Pulse Input to Serial Input Diode and Video Output



The purpose of studying CTE as a function of FZ level is to determine the level that is just adequate to eliminate fixed losses resulting from surface states or other loss mechanisms. A smaller amount of FZ limits low light-level resolution, and a greater amount limits dynamic range without measurably improving resolution. Elimination of fixed loss is determined from the shape of the output waveform. Referring to Figure 5.4, the loss will be purely proportional (no fixed loss) if $v_i = v_i'$ (i = 1, 2, 3, ...). A deviation from this symmetry is indicative of a fixed loss mechanism.

J. SQUARE-WAVE AMPLITUDE RESPONSE

Square-wave bar charts are focused onto the imager with a 55 mm Ultra-Micro-Nikkor, f/2 lens, stopped down to f/8. The magnification of the bar charts is adjusted so that the image of the highest spatial frequency bar chart matches the Nyquist frequency of the imager. The Nyquist frequency of the imager in the x and y directions (rows and columns of the imager) is defined as

$$f_{NYO,x} = \frac{1}{2} d_x$$
, $f_{NYO,y} = \frac{1}{2} d_y$

where d_x and d_y are the pixel dimensions in the x and y directions (noninterlaced). For the device being studied $f_{NYO,x} = 21.9$ line pairs per millimeter.

The square-wave amplitude response (SWAR) is defined as the modulation observed at the sample-and-hold amplifier, for a given spatial frequency square-wave bar chart, i.e.,

$$SWAR = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$$

V is the voltage amplitude of a given pixel at the output of the sample-and-hold amplifier, and V_{max} and V_{min} are obtained by alternately adjusting the phasing between the bar images and the given pixel to obtain first a maximum and then a minimum response. The irradiance level is adjusted so that with uniform illumination the corrected precharge current is in the range $I_{cat}/2 < I - I_D < I_{sat}$. The SWAR for both vertical and horizontal bar patterns is measured in the center of the array. Measurements are made using both wideband and narrowband light.

The effect of the lens on the measured SWAR values can be estimated according to the following procedure. Assume the aperture of a CCD pixel has a rectangular sensitivity function for which the modulation transfer function (MTF) or sine-wave response function is

$$MTF_{aperture}(F) = \frac{\sin[(\pi/2) (F/F_{NYQ})]}{(\pi/2) (F/F_{NYQ})}$$

where F is the spatial frequency of a sine-wave light intensity distribution incident on the pixel. Assume that a square-wave bar chart of spatial frequency F, maximum intensity $l_o + l_1$ and minimum intensity $l_o - l_1$ [i.e., having a contrast $(I_{MAX} - I_{MIN})/I_{MAX} + I_{MIN} = (I_1/l_o)$] is imaged onto the CCD through a lens having a known MTF as a function of frequency. It may then be shown that



SWAR(F) =
$$\left(\frac{I_1}{I_0}\right) \frac{9}{\pi^2} \frac{F_{NYQ}}{F} \sum_{n=1,3,5...}^{\infty} (-1) \frac{n-1}{2} \times \frac{\sin[(n\pi/2)(F/F_{NYQ})]}{n^2}$$

$$\times MTF_{LENS}(nF)$$
(5-1)

Note that the factor $(1/n^2)$ heavily weights the lower frequency MTF values of the lens.

For CCD evaluation a Nikon lens at an f/8 aperture, magnification of 10:1 is used, and for $F_{NYO} = 21.9$ lp/mm we find that

SWAR(F = F_{NYQ}) =
$$\frac{I_1}{I_o} \frac{8}{\pi^2} \left[\frac{0.90}{1^2} + \frac{0.62}{3^2} + \frac{0.40}{5^2} \right] = 0.80(I_1/I_o)$$
 (5-2)

where the experimentally measured MTF values for the lens, with wideband illumination, have been used. A similar calculation for the Wollensak lens yields a response of 0.65 (I_1/I_0). The measured bar chart contrast is greater than 99.9 percent over the range of 0.4 to 1.1 microns, so the factor (I_1/I_0) can be taken as unity in Equation (5.2).

Note that a large loss in square-wave amplitude response is incurred because of the lens. If the bar chart contrast is 100 percent, i.e., $I_1 = I_0$, an aperture with a square aperture response function and having the same dimensions as a pixel would only show an 80 percent (65 percent) SWAR at the Nyquist frequency because of lens degradation, whereas if the lens were perfect, the SWAR would be unity out to the Nyquist frequency, dropping to zero at twice the Nyquist frequency.

Rather than establish an upper limit for the response of an idealized aperture, we might try to correct directly the SWAR data for the lens degradation. If sine-wave response were being measured, the sine-wave response of the CCD could be found by simply dividing the measured sine-wave response by the sine-wave response (or MTF) of the lens. For square-wave amplitude response measurements, the procedure is more difficult since a summation of sine-wave response products must be inverted. Referring back to Equation (5-1), we have

SWAR(F) =
$$(4/\pi)\sum_{n=1,3.5...}^{\infty} (-1)\frac{(n-1)}{2}(1/n)MTF_{lens}(nF) \times MTF_{CCD}(nF)$$
 (5-3)

where the square aperture response approximation has been replaced by the actual MTF of the CCD, and the contrast of the bar chart has been set at 100 percent.



Equation (5-3) may be inverted to yield a value for $MTF_{CCD}(F)$, $MTF_{CCD}(3F)$, ..., which can be used to give

SWAR_{CCD}(F) =
$$4/\pi \sum_{n=1,3,5,...}^{\infty} (-1) \frac{(n-1)}{2} (1/n) MTFCCD(F)$$
 (5-4)

The inversion, however, requires experimental values for SWAR(F), SWAR(3F),

The actual procedure for measuring the square-wave amplitude response is to motor drive a bar chart past the lens, and sample-and-hold a given pixel amplitude from one frame to the next. The sample-and-hold output is displayed on an X-Y recorder. The result is a plot of the modulation produced by the bar chart at the given pixel of interest. The bar chart consists of 11 sets of bars of different spatial frequencies produced by a Gerber plotter in the photomask area of Texas Instruments.

Measurements are not made with a fixed bar chart for several reasons:

- If the device has an SWAR gradation across the image area (a common property of charge-transfer devices), a fixed bar pattern precludes a purely local measurement from being made. This is usually a small effect unless there are open clock lines leading to sudden discontinuities in SWAR.
- A fixed bar pattern can lead to the modulation pattern being distorted by blemish pixels or slower response variations.
- In addition, at frequencies near the Nyquist frequency, the phasing of the bar chart with respect to the CCD pixels must be varied in order to maximize the modulation, which means that at the very least the bar chart must be moved manually.
- With the addition of special sample-and-hold electronics, a moving bar chart can lead to an accurate, automated plot of the SWAR of a given pixel.

K. RESIDUAL IMAGE

Residual image measurements are made by imaging a high-contrast bar chart that is strobed with a xenon flashtube during one integration period. The resulting image is read out of the CCD. During the next integration period the device is kept unilluminated. After this integration period has ended, the device is read out and any trace of the bar chart pattern constitutes a residual image. Line and frame photos of the first and second readouts are taken from an oscilloscope to quantitatively record the images.

L. MEMBRANE PLANARITY

Membrane planarity is measured by a Zeiss flatness tester using a $0.624 \,\mu m$ laser source or interference microscope with a $0.56 \,\mu m$ source. The Zeiss tester is basically a large field-of-view Fizeau interferometer. The field of view is variable from $\frac{1}{2}$ to 3 inches.



The reference mirror of the flatness tester is adjusted to give the minimum number of fringes, a condition which makes the membrane perpendicular to this mirror on the average. Under this condition, the fringes form closed loops of decreasing dimension where the point about which the loops collapse is the highest (or lowest) point on the membrane. If N fringes are counted from this point to the edge of the active area of the CCD, then the membrane planarity is

planarity =
$$\pm N\lambda/4$$
 (5-5)

The Zeiss flatness tester is being modified to give a greater working distance between the reference mirror and the CCD to investigate the possibility of planarity measurements of devices which are cooled inside the environmental camera. The double-window assembly of the camera requires about 1.5 inches of working distance, whereas the present working distance of the flatness tester is 0.1 inch. A greater working distance will be accomplished by replacing the incoherent cadmium source with a coherent, beam expanded, helium-neon laser source. This will have the additional advantage of more clearly defined fringes since the helium-neon laser line is extremely narrow compared to the cadmium source.

For the 400 X 400 arrays the variation from membrane center to edge amounts to about 2 mils. Using the interferometer to observe the fringe pattern results in very closely spaced fringes which are difficult to count. Several nonoperating 400 X 400 arrays were thinned, then coated from the front side with epoxy. This stiffens the membrane and allows a mechanical probe (Talleystep) to be moved across the surface in order to measure flatness. This allows an estimate of results using similar thinning technology on defect-free CCDs.



SECTION VI CCD OPTICAL CHARACTERISTICS

A. GENERAL IMAGING

The performance of thinned CCD images was extensively studied both at 24° C and -40° C. Repeated cycling between these temperatures has never resulted in device failure. The devices studied were all mounted to the ceramic headers using room-temperature epoxy. The first 100×160 tested had epoxy completely covering the front of the array for membrane support. This resulted in cracking of the membrane at -20° C and was immediately abandoned.

Detailed parameters measured on the arrays delivered to JPL are given in the appendixes to this report. These tests were designed to allow some insight into operation of the devices at the low data rate (10 kHz) and long exposure times required in the original contract. Initially, it was desired that all measurements be made at -40° C and 10 kHz. Early in the program it was demonstrated that some parameters were unchanged in cooling from 24° C to -40° C and were more easily measured at 24° C. In such cases, later measurements were performed only at 24° C. These types of measurements are spectral response, CCD signal versus light intensity, and square wave amplitude response; each is discussed separately below.

Figure 6-1 shows monitor photographs of imagery taken with a 100 X 160 array and a 400 X 400 array. The experimental apparatus used a strobe (pulse $\sim 5 \,\mu s$) to illuminate a positive print of the IEEE Standard. This target is chosen because of the many gray shades. The object is focused on the CCD by a lens and, after the strobe pulse, the CCD is read out in the dark to simulate a shuttered mode of operation. The video display on the monitor is adjusted to give about the same size display for each sensor. The lines in the 400 X 400 are just blurred into each other and are not visible in Figure 6-1. A Polaroid MP4 camera is used to photograph the TV monitor. The 400 X 400 shows two types of defect which are common in CCD fabrication. The first is a partially blocked parallel channel. Thus, information above it cannot be transferred to the output and a black line results (upper right of photograph). The second type of defect is a dark-current spike. Here it is streaked over an entire column. The data rate is 1 MHz and at 3 MHz data rate the spot is isolated to a few pixels. The resolution of the image is extremely good and no degradation is seen at points far from the CCD output. Such results (JPL 11, Appendix D) indicate very high parallel CTE.

Figure 6-2 shows imagery taken at -40°C. It appears that the CTE of the array is unaffected by temperature between 24°C and -40°C. In A, Figure 6-2, the data rate is 1 MHz and the dark-current generation is reduced in the blemished pixel so it can no longer be detected in the photograph. In B, Figure 6-2, the data rate is 10 kHz, corresponding to a frame time of 16 seconds. During this time, the number of electrons generated in the blemished area are contributing to each charge packet as it transfers through that area and so results in the white line across the array. The reason that these photographs show the white line both above and below the defect site is because several frames have been integrated by the camera. A single frame should only generate a white streak from the defect site to the top of the array. For the 10 kHz readout an electronically controller shutter over the Dewar window was used to keep the array in the dark. If the array is not shuttered, that is, light falls on it during charge transfer, the well population does not reflect the true object exactly because each transferring packet sees a



T = 24°C STROBED ILLUMINATION

160 X 100

400 X 400



FRAME TIME 163 MILLISECONDS

FRAME TIME 16 MILLISECONDS

194265



1 MHZ - 40°C FRAME TIME 163 MS



(B) 10 KHZ - 40°C FRAME TIME 16 SEC

Figure 6-2. Imagery at -40°C Taken at 1 MHz (A); and 10 kHz (B)



contribution from other parts of the object. For example, if a black and white bar chart were maged across the parallel channels and read out while illuminated, the black, i.e., empty pixels, will pick up some charge as they are read out through an illuminated area. Thus, some contrast is lost and an image appears streaked. To achieve an image (for example, the IEEE Standard that does not appear streaked when continuously illuminated, a ratio of integration time to readout time of 3:1 is recommended.

The appearance of an image taken with a CCD depends strongly on the conditions under which it is taken. For example, consider the case of an imager characterized by high concentration of dark-current spikes. If a picture is taken with very short integration time, i.e., short flash and high intensity illumination followed by a fairly rapid readout, the dark-current sites may not fill up appreciably with electrons and the image will look relatively defect free. If, however, the scene is illuminated at low light levels, the device must integrate for longer periods to build up signal charge. However, all the defect sites now have an increased time to generate spurious electrons so that after readout, the defects are quite obvious. A photograph taken with an imager which had a number of localized defects is shown in A, Figure 6-3. Here, the array is strobe illuminated and then allowed to remain in the dark for 16 seconds before readout at 1 MHz. The defects have had time to build up appreciably in the 16-second frame time and appear localized. If such an array was strobe illuminated and read out immediately, only the single bright line would be visible. The black line is constant since it is due to a blocked channel. B, Figure 6-3, shows the image if the object is strobed and then the CCD is read out immediately but at 10 kHz. The frame time is therefore the same as in A, Figure 6-3. The localized defects are not apparent since time is not allowed and the defect sites are continually emptied as each packet transfers through it.

The capability of the arrays at low light levels was briefly investigated. To achieve good imaging at low levels, uniform dark current and good uniformity of response is required. Figure 6-4 shows a series of pictures taken from the monitor for different light levels as controlled by neutral density filters. From knowledge of the full well electron population and the neutral density filters used, it is straightforward to determine the number of electrons on one pixel. It is quite easy to pick out the detail on the bar chart at a level of 300 electrons.

During the initial characterization of imagers in the program it became apparent that the devices were producing alternate light and dark lines on the monitor for uniformly illuminated objects. This line pairing effect is shown in A, Figure 6-5, where an oscilloscope display of several lines is presented. The magnitude of the line-to-line variation was a function of operating potentials and could be minimized to not less than about 5 to 10 percent by appropriate optimization. This is illustrated by video dark-current signatures taken with operating potentials shown in C, Figure 6-5. This artificial nonuniformity was undesirable from any systems application viewpoint. As pointed out in Section II, a feature of the 3ϕ CCD double-lvel CCD is that a given phase, for example, ϕ_1 in the parallel section, occurs under a 1st, 2nd, 1st, 2nd . . . electrode.

Since ϕ_1 is held high to integrate charges in the parallel section, any small differences in collecting silicon area will be reflected in a series of lines which are high, low, high, low. To test the idea that differences between first and second level electrode areas give the pairing, the parallel integration is done using $\phi_2 + \phi_3$ so that the integrating cell also is always composed of a 1st and 2nd level electrode. This is shown in B. Figure 6-5, where it is clear that the line pairing is eliminated. The data shown in A. Figure 6-6, is the square-wave amplitude response taken using first line 51, bit 80, then line 52, bit 80, with integration under ϕ_1 only. Then





(A)
1 MHZ DATA RATE
16 SEC STORAGE
FRAME TIME 16 SEC



(B) 10 KHZ DATA RATE 2 MS STORAGE FRAME TIME 16 SEC

Figure 6-3. Comparison of Long Storage (A); and Rapid Readout at 1 MHz With Long Readout at 10 kHz (B)



integration is changed to $\phi_2 + \phi_3$ and the SWAR recorded on line 51 or line 52, bit 80, with the same results. Note that the $\phi_2 + \phi_3$ data appears more uniform and averages the results using just ϕ_1 integration. It appears that $\phi_2 + \phi_3$ offers improved reproducibility in the SWAR measurements.

B. DARK CURRENT

The signal charge in a CCD imager consists of photogenerated electrons stored and transferred in depletion wells created by voltage applied to the electrodes of the CCD. For a surface-channel device the electrons interact with surface states since storage occurs at the surface and, for a buried channel device, signal electrons interact predominantly with bulk states. The potential wells accumulate thermally generated electrons from centers in the bulk and at the surface. These charges, as well as using the available storage capacity of the well, are usually generated from a nonuniform distribution of generation centers. The magnitude of the effect can be seen from the dark-current charge

$$N_{DC} = 348 J_D (nA/cm^2) \frac{T_{int (ms)}}{33} \left(\frac{A cm^2}{1.7 \times 10^{-6}} \right)$$

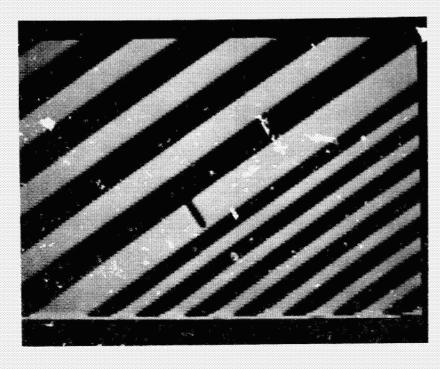
For the 100 X 160 and 400 X 400 array the electrode area is 0.3×0.9 mil = 1.76×10^{-6} . Therefore, for any array dark-current density J_D , the number of electrons generated under a single integrating electrode during the integration peric 1 can be calculated. Typical full well for the CCD imagers is 5×10^5 electrons.

J _D (nA/cm ²)	N _{DC} Electrons (in 33 ms)	Time to Full Well
100	3.48 104	0.47 s
50	1.74	0.94
20	6.96 103	2.35
10	3.48	4.7
5	1.74	9.4
2	6.96 10°	23.5
1	3.48	47.0 s

To achieve these storage times in practice with an area CCD imager, it is required that there are no localized sites of very high generation rate which will allow the dark charge to spread across the large area of the array (i.e., bloom). Also, no spurious effects are required such as carrier generation beneath channel stops, carrier generation due to avalanching near the channel stops, or from areas near the output amplifiers which are locally heating the CCD.

Several mechanisms contribute to dark current.¹⁸ The intrinsic generation rate, U_i , due to band-to-band transitions in silicon is $U_i = n_i/\tau_i$ where n_i is the intrinsic carrier concentration and τ_i the electron lifetime. Assuming $n_i = 1.6 \times 10^{10}/\text{cm}^2$, $\tau_i = 2.5 \times 10^{-3}$ second and a depletion layer width, x_d of 3 μ m gives

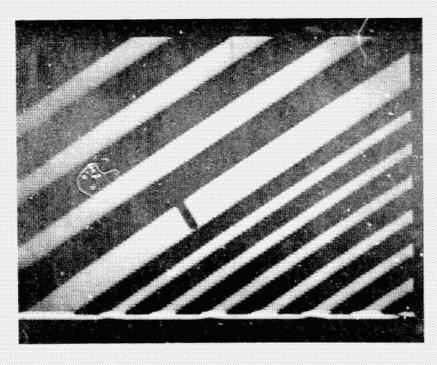
$$I_1 = q \frac{n_i}{\tau_i} \quad x_d \sim 0.3 \text{ nA/cm}^2$$





A. 1 X 10 ELECTRONS/PIXEL

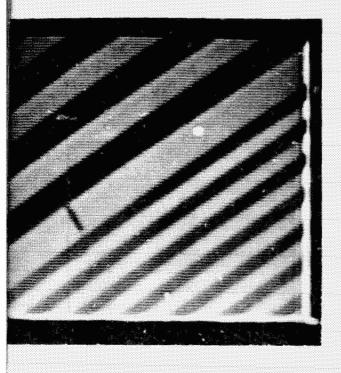




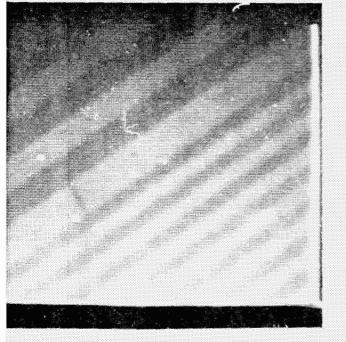
B. 1 X 10 5 ELECTRONS/PIXEL

D. 3

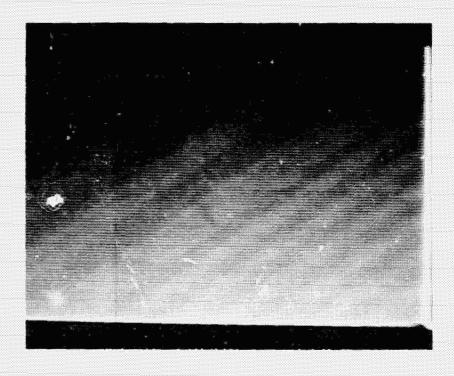




C. 1 X 104 ELECTRONS/PIXEL



D. 3400 ELECTRONS/PIXEL

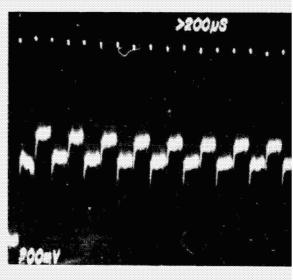


E. 1000 ELECTRONS/PIXEL

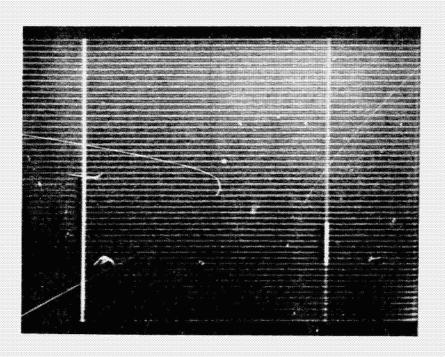


F. 340 ELECTRONS/PIXEL

Figure 6-4. Photographs of Bar Chart Focused on 100 X 160 CCD For Different Electron Population In Each Pixel

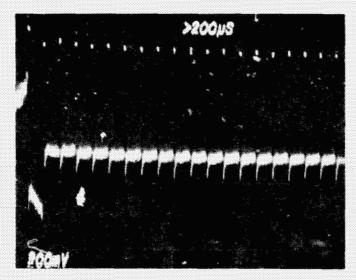


 $\Sigma_{t}\phi_{t}$

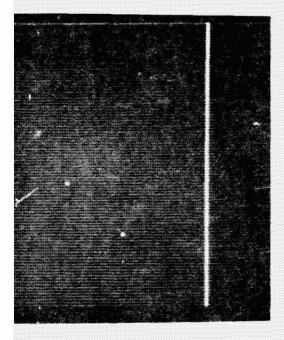


SUB OV CLOCKS 6V

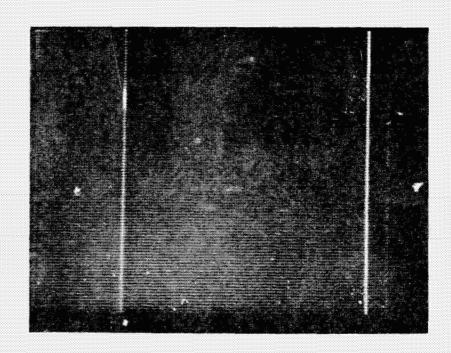




 $\Sigma_{1}\phi_{2}\,\phi_{3}$



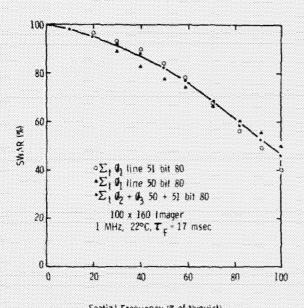
SUB -1V CLOCKS 6V



SUB -1V CLOCKS 8V

Figure 6-5. Line Pairing When a Single Parallel Phase Is Used For Integration (A); and Zero Pairing If Two Phases Are Used (B)





Spatia 1 Frequency (% of Nyquist)

194270

Figure 6-6. SWAR Data For Cases (A) and (B) of Figure 6-5 Shoring Improved Reliability for Data With Two lutegrating Phases

Carriers from the neutral bulk can diffuse to the depletion region giving

$$I_2 = \frac{qn_1^2}{N_A \tau_n}$$
 $E_n \sim 0.075 \text{ nA/cm}^2$

where $N_A \sim 10^{15}$ cm⁻³, the electron mobility $\mu_n = 1.200$ cm²/volt/second, $\tau_n = 1 \times 10^{-4}$ second and $L_n^2 = D\tau_n = \mu \tau_n kT/q$.

Bulk generation of electrons in the depletion region is from g-r centers and can be expressed

$$I_3 = \frac{1}{2} q n_i v_i \sigma_b N_i x_d$$

where v_t is the thermal velocity, σ_b the capture cross section of the states of density N_{ss}. Using $\sigma_b = 2 \times 10^{-16}$ cm² and $\tau_n = 100 \,\mu s$ (N_t = 5 × 10^{12} cm⁻³)

$$I_3 = 3.9 \text{ nA/cm}^2$$

Surface states can also generate dark current. This contribution is

$$I_4 = \frac{1}{2}qn_1\sigma_s v_1\pi kTN_{ss}$$

where σ_s can be from 1×10^{-14} to 1×10^{-16} and N_{ss} can be as low as 2×10^9 with optimum processing. For $\sigma_s = 10^{15}$ and $N_{ss} = 2 \times 10^9$

$$I_4 = 2 \text{ nA/cm}^2$$

From these figures it can be seen that the dominant sources of dark current will be due to surface and bulk generation sites. The temperature dependence of the dark current will be determined by the temperature dependence of n_i which is well known and $\alpha T^{3/2} \exp(-E_g/2kT)$, where E_g is the silicon energy gap. The $T^{3/2}$ reflects the density of states effect. The commonly used approximation of a decrease in J_D by a factor of 2 for every $10^\circ C$ change on temperature is only valid around $24^\circ C$ and gives a very poor result if used between -40° and $+24^\circ C$. A plot of this equation is given in Figure 6-7. A decrease of about $1050\times$ is predicted between $25^\circ C$ and $-40^\circ C$.

Experimentally, the CCD dark current has decreased in magnitude throughout the program. Early buried-channel arrays showed dark current from 20 to 60 nA/cm². JPL 6, a buried-channel array delivered in December 1974, showed a lower value of 7.8 nA/cm² at 24°C. By mid-1975, the technology had developed so that J_D close to 1 nA/cm² was observed for a significant number of smaller 100 X 160's and in several 400 X 400's.



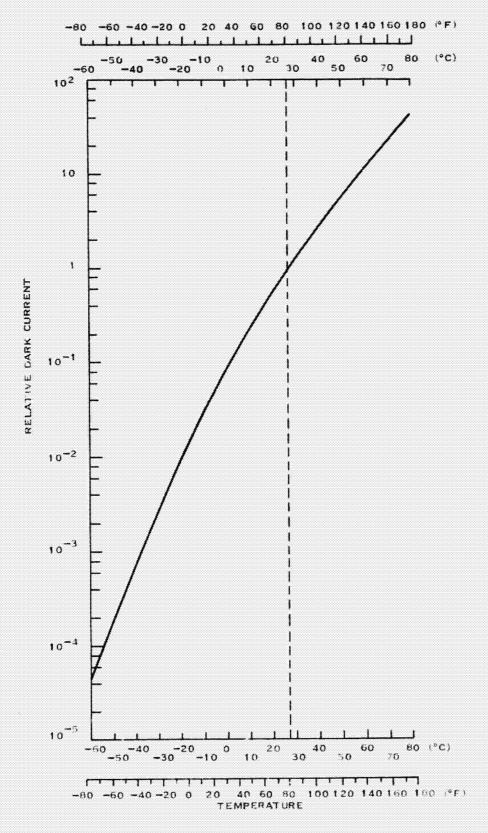


Figure 6-7. Theoretical Variation of CCD Dark Current With Temperature



One of the contributing factors to the total dark current of an array was determined to be dependent on the bias of the load MOSFETs on the BSHA and CCA. The effect appeared to be due to heating of the thin CCD membrane by the power dissipated in the amplifier MOSFETs. Thus, the area around the two output corners of the array is at a higher temperature than the rest of the membrane. As a result, the dark current is higher in these areas. There are four active MOSFET loads in the BSHA and four source-follower MOSFETs; under bias the power dissipated was about 150 milliwatts. The effect of this is shown in Figure 6-8. The bias voltage on the load MOSFETs is V_{gg} and the resistance of this load is a function of V_{gg} . Decreasing V_{gg} results in a reduction of the bright areas on each corner of the array which are areas of locally higher temperature. The value of V_{gg} cannot be reduced indefinitely, however, and usually the lowest was used for array operation consistent with operation of the follower with an adequate bandwidth. The contribution of this heating toward filling the potential wells of the CCD increases with the time during which the device is held in the integrating mode. For example, a rapid 1 MHz data rate and integration times in the tens of milliseconds regime did not allow a significant buildup of dark charge anywhere in the array. However, for long exposure times of say, 5 seconds at -40°C, followed by MHz readout (0.16 s) or 10 kHz readout (1.6 s), the dark charge generated near the amplifiers would result in a significant spurious well population. With increasing time, the dark charge would initially saturate the CCD in the corners and then spread into the array. The effect on average dark current is shown in Figure 6-9. In this experiment the Vgg is gated off during the integration period so that there are no spurious amplifier effects during this period. The amplifier is then gated on during readout. The average dark current is a strong function of the ratio of τ_{ro} to τ_{i} , and approaches the true value of array dark current at long τ_i . Two cases are shown. The first is data taken with the 100 X 160 in a static ambient (atmosphere) and the second with room-temperature nitrogen blowing around the device. In the first case, the device temperature appears to be uniformly increased from ambient. Note the significant increase in J_D due to heating from the long τ_F value of ~0.7 nA to 3.2 nA with continuous readout. This mode of operation was, of course, not particularly effective at 10 kHz data rates since the readout time is necessarily long and array performance is limited. The magnitude of the effect depends on the location of the output amplifier with respect to the thin membrane. In Figure 6-9 the amplifier is about 15 mils onto the thin membrane away from the thick silizon rim. Such a large window results in better intrinsic uniformity from the thinning process but much stronger heating due to the high thermal impedance. Positioning of the amplifier on the thick silicon gave less apparent heating due to the large mass of silicon present to dissipate the heat.

Because of the problem of localized dark current, the amplifier on the 400 X 400 was designed with no on-chip load MOSFETs. There will still be, however, some 20 milliwatts of power dissipated on-chip due to a drain current of ~2 mA and a source to drain voltage about 10 volts. V_{ds} may be able to be reduced further for a su face-channel MOSFET but some power must be generated and this will lead to a (much smaller) temperature rise in the neighborhood of the output corners of the array. It was expected that because of the low data rates required for eventual array operation, a higher value of source-follower load resistor, R_L than normally used (50 kilohms versus 4.7 kilohms) would further decrease the amount of power generated in the follower MOSFET. Use of a 50 kilohm external load with the 400 X 400 appears to reduce the heating to less than 2°C of ambient while maintaining a bandwidth through the follower of about 1 MHz. The dark-current uniformity also increases if the heating effect is eliminated. Note, however, that variations in dark current become progressively less important as the magnitude decreases.





A. V_{gg} = 17.5 VOLTS V_{dd} = 24 VOLTS 1 MHZ PRODUCED HEATING AT THE AMPLIFIER CORNERS OF THE ARRAY

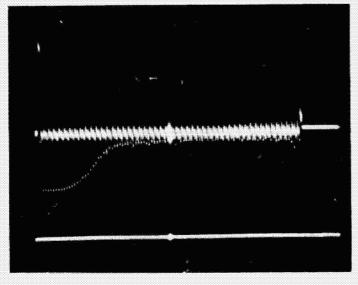


B. Vgg = 8 VOLTS

Vdd = 24 VOLTS

1 MHZ

HEATING REDUCED CONSIDERABLY



C. ONE FRAME
1 MHZ
SHOWS HEATING EFFECT
1S STRONGER FROM THE
LOWER AMPLIFIER

Figure 6-8. Effect of Gate Bias on Load MOSFET on Array Dark Current



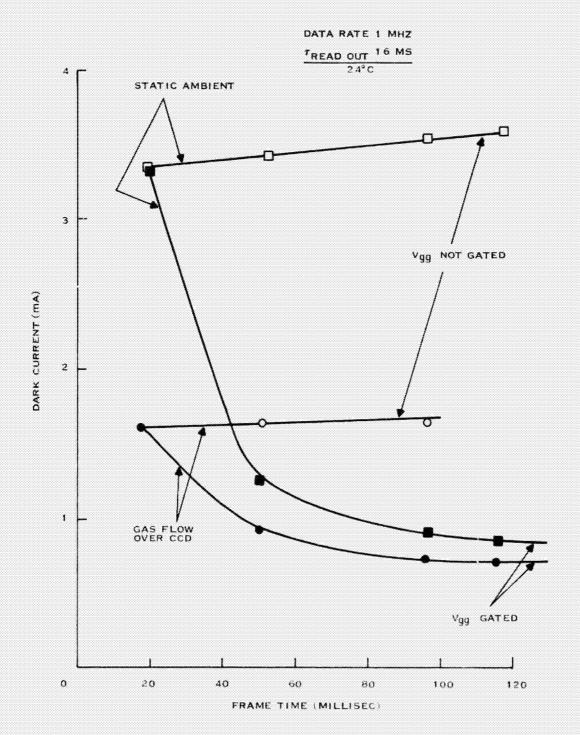


Figure 6-9. Variation of Average Dark Current Measured in the Precharge Line With Frame Time



One of the most impressive results of the technology is the magnitude of the storage time achieved in the CCDs at 24° C at the end of this phase of the JPL program. This is measured by illuminating a device with a strobe and then allowing it to rest in the dark for a time, t_s , prior to the information being read out. Figure 6-10 shows the results of such an experiment at 24° C where values of t_s are given. For this particular device, 10-second storage results in some potential wells filling but the image is still clearly detectable. In addition, the dark current is extremely uniform with magnitude of 1.3 nA/cm^2 . Any localized defect regions will bloom at long storage times in such a test so that the data of Figure 6-4 reflect both magnitude and uniformity. The highlights in the Figure 6-4 data were maintained at 40 percent full well so the maximum storage time is the time to fill the remaining 60 percent of the well capacity. For this experiment $R_L = 50 \text{ k}\Omega$ and, in addition, the source follower was gated off during the storage period to completely eliminate heating effects. The effect of amplifier heating is small, however, in this case.

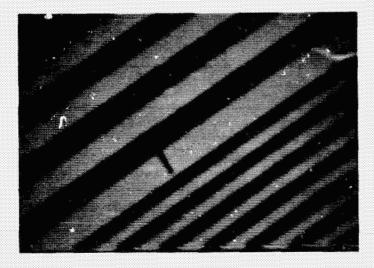
Two characteristics of the area imagers which are important in operation of the devices are the magnitude of the dark current at -40° C and the dependence of dark current on clock voltage.

The temperature dependence of the dark current is especially dependent on the heating effect. This can be seen from Figure 6-1 where a 1°C temperature rise at -40° C gives a larger increase in J_D than a 1°C rise at 24°C ambient. To observe the intrinsic variation of J_D , heating should be negligible at all temperatures and, for early arrays, this was not the case. For the 400 X 400's and later 100 X 160's, 50 kilohm external load resistors were used in such measurements and the experimental results confirm very closely the expected intrinsic dependence. These measurements are given in A, Figure 6-11, and were taken by sampling all 160,000 pixels of a 400 X 400 using the multichannel analyzer. The dark current is obtained from the peak of the (approximately) Gaussian distribution, ignoring the few highly blemished defects in the array. Note that the magnitude of the dark current at 24°C is 0.9 nA/cm and at -40° C is 1 pA/cm^2 . In this experiment the array is read out at 1 MHz. At low data rate (10 kHz), particularly for some of the smaller arrays, the heating effect at the output during the readout time results in higher dark current than expected at -40° C. This contribution can be large, particularly with low source-follower resistors since the amplifier is usually well into the thin silicon for the 100 X 160.

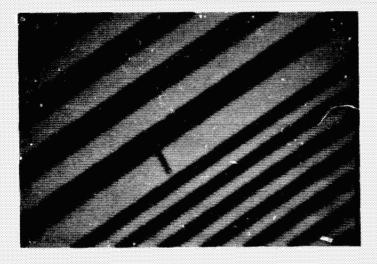
The temperature dependence of the dark current is also a sensitive measure of the quality of the array itself. We have observed that in regions characterized by high dark current (localized dark-current spikes) the magnitude of J_D does not decrease with temperature as rapidly as in neighboring defect-free regions. In some cases these spikes are essentially independent of temperature. As a result, the average dark current will saturate at some level as the temperature is decreased depending on the density of these "impurity sites." Such effects have also been reported elsewhere. A second cause of anomalous temperature dependence can occur if attempts are made to measure average dark-current with a picoammeter rather than using the integration technique described in Section V. While this average measures the spikes also, the dark current for good arrays is so small that it is indistinguishable from various de leakages on the CCD header.

The second characteristics of importance is the dependence of dark current on the clock voltage required to transfer charge. If the array dark current is dominated by bulk generation centers, it is expected that the dark current will increase as $V_{CL}^{\frac{1}{12}}$ because of the increase in





A. 1 MHZ FRAME TIME 45 MS



B. 1 MHZ STORAGE 5 SEC



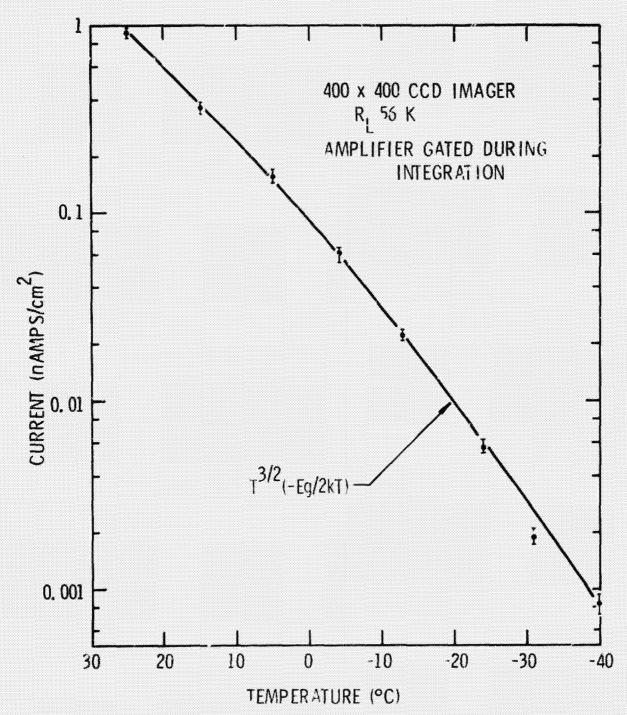
C. 1 MHZ STORAGE 10 SEC

194274

Figure 6-10, 24°C Storage With a 100 X 160 Imager Showing Excellent Imaging at 10 Seconds.

This is Equivalent to About 2nA/cm² Dark Current,

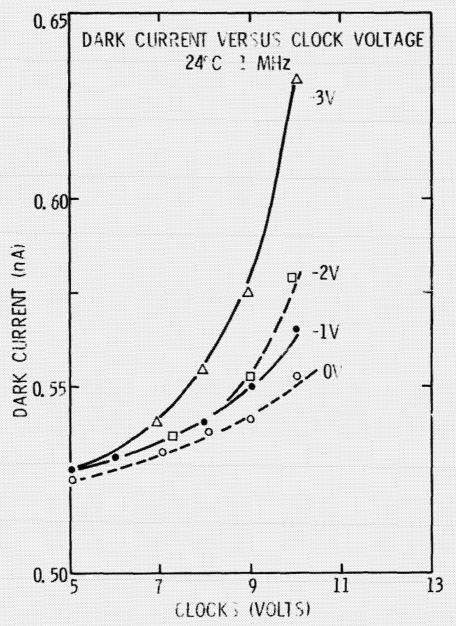




A. COMPARISON OF DARK CURRENT FOR A 400 X 400 WITH EXPECTED TEMPERATURE BEHAVIOR

Figure 6-11. Characteristics of Dark Current for CCD Arrays (Sheet 1 of 2)





B. DEPENDENCE OF ARRAY DARK CURRENT ON CLOCK VOLTAGE FOR SEVERAL SUBSTRATE BIAS VALUES

Figure 6-11. Characteristics of Dark Current for CCD Arcays (Shec ... of 2)



depleted silicon. If surface generation dominates, a much smaller dependence on V_{C1} would be observed. A rapid increase of dark current at some clock voltage may signal carrier generation from an avalanching reverse-biased junction between the p^+ channel stop and n layer. It is observed that array dark current of buried-channel imagers is essentially independent of V_{C1} , the parallel clock voltage (B, Figure 6-11). Park current increases with substrate bias.

It is expected that both contributions will scale with temperature a n_i in agreement with the experimental data of A, Figure 6-11.

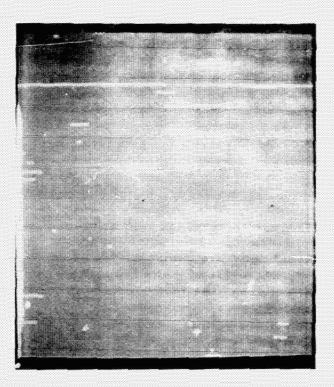
As indicated in Section III, some 400 X 400 processing was performed on 3-inch silicon slices. Although the process sequence was very close to identical to that successfully used for 2-inch processing, some unavoidable differences were present. A result of these differences can be seen by comparing A and C, Figure 6-12. These show monitor displays of the dark current from two types of 400 X 400 imagers at 24°C. In A, Figure 6-12, the low dark current devices are typified and integration of 1 second is used to show up any defects at all In C, Figure 6-12, the localized blemishes show up at 163 milliseconds. Cooling to -40°C is shown in B and C, Figure 6-12. In C, Figure 6-12, it is clear that not all spikes have decreased with temperature in the same manner. Several areas are suspect and may account for the differences shown above. It appears that cleaning techniques in the 3-inch processing may damage the slice to a greater extent. Also, the silicon nitride and gate oxides are grown using slightly dissimilar techniques. These differences are being investigated in more detail.

Recent results obtained by JPL using a 100 X 160 array after this manuscript was written indicated that the 'heating' effect has a sharp 'threshold' and is removed by reducing $V_{\rm ds}$. Thus, it seems there may be some form of localized breakdown at the source follower causing the increased number of electrons near the output. Nevertheless, the spread of the apparent heating effect, which can be detected across a 100 X 160, i.e., 0.14 inch from the amplifier seems more consistent with heating due to this breakdown rather than diffusion of generated carriers out from the region of the amplifier. This is an area of current investigation.

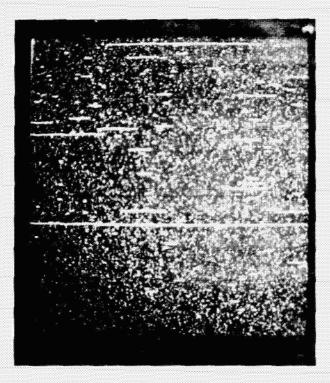
The uniformity of dark current, once amplifier effects are eliminated, is excellent. Uniformity, pixel to pixel can approach 5 percent. A video output trace from a 100 X 160 array which has been allowed to integrate at room temperature to fill the wells to about 50 percent is shown in Figure 6-13. The uniformity for the 400 X 400 is essentially the same. Note the increase in dark current at the end and at the beginning of the line. This seems fairly typical and may represent enhanced generation due to the strains induced at the thin/thick silicon transition, i.e., the edge of the thinning window.

Because of the very low dark current of the 400 X 400, information can be stored for extremely long storage times at -40°C. Figure 6-14 shows the video output from a 400 X 400 in a similar experiment to that described earlier (Figure 6-10). The essential difference is that the 400 X 400 has several localized defects which eventually bloom down the parallel channels as the dark charge builds up with longer storage time. In 78 minutes these spikes result in complete blemishing of several channels but in adjacent regions the well population is still only about 30 percent. Time to full well in these areas is estimated to be about 3 hours. It is very difficult to make defect-free 400 X 400's due to the physical size. Thus, imaging at very long times will result in several saturated lines (as shown in Figure 6-14). Improved technology will eliminate this effect. Imaging at long storage times is shown in Figure 6-15 for a 100 X 160, which, with





A. 24°C, τ_F = 1 SEC, LOW DEFECT



8, 24°C, 7 = 163 MS, HIGH DEFECT

Figure 6-12. Dark-Current Signature of a Low Defect 400 X 400 Array (Sheet 1 of 2)





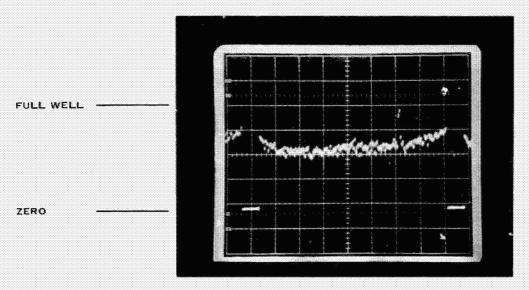
c. -40°c. τ_F = 1 SEC. LOW DEFECT



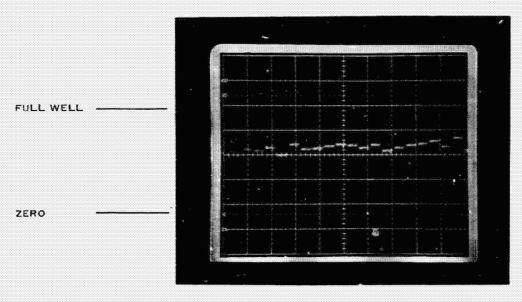
D. -40°C, $\tau_{\rm F}$ = 163 MS, HIGH DEFECT

Figure 6-12. Dark-Current Signature of a Low Defect 460 X 400 Array (Sheet 2 of 2)





A. AFTER INTEGRATING 10 SECONDS TO REACH 50% FULL WELL



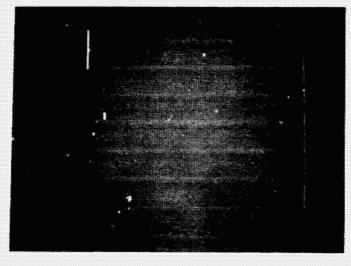
B. PIXEL UNIFORMITY ON EXPANDED TIME SCALE, SAME VERTICAL SCALE

Figure 6-13. Typical 24°C Dark-Current Uniformity of a Line From a CCD Imager

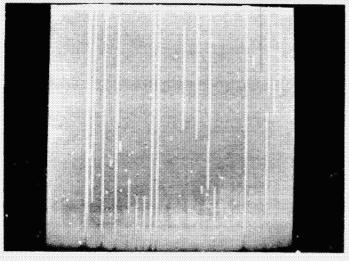




-40° STORAGE 0.75 SEC 1 MHZ DATA



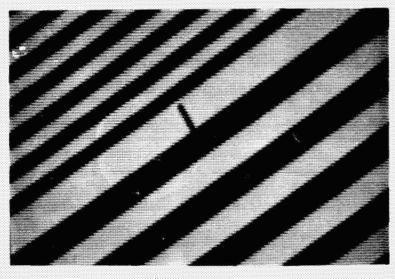
-40° STORAGE 18 SEC 1 MHZ DATA



-40° STORAGE 78 MIN 1 MHZ DATA

Figure 6-14. Dark Current Signature From a 400 X 400 Allowed to Integrate For Up to 78 Minutes Prior to Readout of the Data at 1 MHz at -40° C

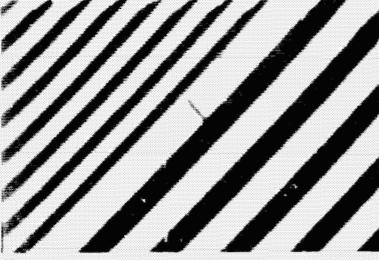




-40° STORAGE 16 MS



-40° STORAGE 10 MIN



-40° STORAGE 96 MIN

Figure 6-15. Imaging With a Bar Chart Using a 100 X 160 Array at -40°C Showing Storage Times of 96 Minutes Without Significant Image Degradation



current technology, can be made defect-free with relative ease. Excellent imaging is seen up to 96 minutes storage and it is estimated that several hours will be required to reach full well. The dark current at -40° C for this array is 2 pA/cm^2 .

C. QUANTUM EFFICIENCY AND SPECTRAL RESPONSIVITY

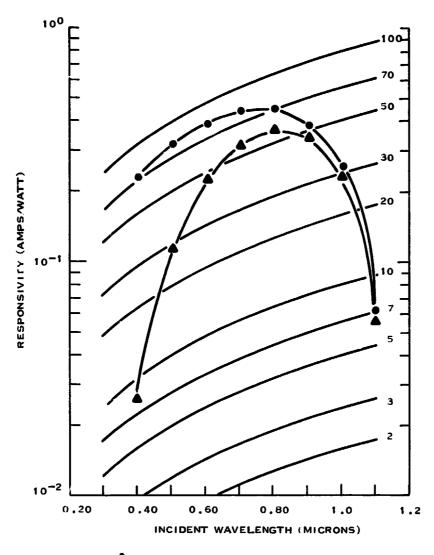
The response of a backside-illuminated CCD imager to incident 2854°K optical radiation is at least a factor of 2 higher than front-side illuminated devices due to the fact that the complete backside surface absorbs incident light. The spectral responsivity to such broadband radiation is in the range 70 to 90 mA/watt. The responsivity peaks at about 8000 Å, where the narrowband response is 380 mA/watt, which is equivalent to a 65 percent quantum efficiency. At longer wavelengths responsivity falls because the absorption coefficient is decreasing rapidly. By 1.1 μ m, response is down to a quantum efficiency of 5 percent. At wavelengths shorter than the peak, the incident radiation is absorbed closer to the surface of the silicon membrane until at λ = 4000 Å the absorption length is about 0.2 μ m. The response at 4000 Å is thus a strong function of surface condition and the p⁺ backside accumulation profile. An excessively thick region results in low response because all photoelectrons are created in a layer with low minority carrier lifetime, therefore, electrons cannot diffuse to the depletion wells. No boron concentration gradient can allow the energy bands to be bent by absorbtion of a surface layer, possibly into inversion, which would also result in low response as photoelectrons would be repelled from the bulk silicon. The optimum is a boron gradient which can drift carriers into the bulk but with a sufficiently low surface concentration (or sufficiently thin high concentration at the surface) to avoid having a sink for the carriers. If this accumulation is carried out in an optimum fashion, it is possible to achieve an essentially flat quantum efficiency if about 65 percent from 7500 Å to 4000 Å. JPL 6 (Appendix A) shows such a response out to 4000 Å. Such a high quantum efficiency is difficult to achieve reproducibly, however, with technology as it exists. A quantum efficiency which is more reliably achieved is in the range of 10 to 30 percent. These results are shown in Figure 6-16. This data is uncorrected for reflectivity losses and the membrane is not intentionally given any antireflection coating. It appears possible that the light haze seen on some thinned membranes may be modifying the reflectivity from the bulk (or cleaved) silicon value.

The spectra shown in Figure 6-16 are free of the structure due to interference effects in front-side illuminated CCD imagers. There are, however, interference effects at longer wavelengths due to multiple passes of the radiation in the membrane itself.

The spectral response of a CCD imager is not expected to depend on temperature between -40° and 24° C, since the change in the silicon energy band gap is quite small. $dEg/dT \cong -2.4 \times 10^{-4} \, eV/^{\circ}$ K so that $\Delta Eg = 15 \, meV$ for $Eg = 1.2 \, eV$, i.e., about 0.1 percent. This independence is observed experimentally (Figure 6-17). In some cases it was observed that the relative response across an array at short wavelengths (4000 Å) would show some variation with cooling to -40° C. This reflects some type of surface instability and was generally not observed on devices showing quantum efficiency in the 10 to 30 percent range. Nevertheless, devices should be stored in a dry ambient to avoid moisture effects.

A second important characteristic of an area imager is the relation between response $J-J_D$ and incident 2,854°K optical radiation.

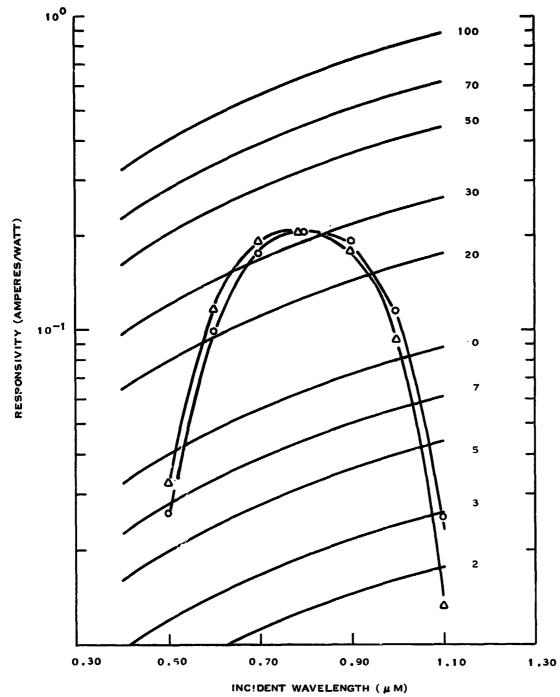




- A. A FOR OPTIMUM ACCUMULATION OF BACKSIDE SURFACE
 - TYPICAL RESPONSE

Figure 6-16. Spectral Response (Sheet 1 of 2)





B, DATA FOR 24°C AND -40°C SHOWING ESSENTIALLY IDENTICAL RESPONSE

Figure 6-16. Spectral Response (Sheet 2 of 2)



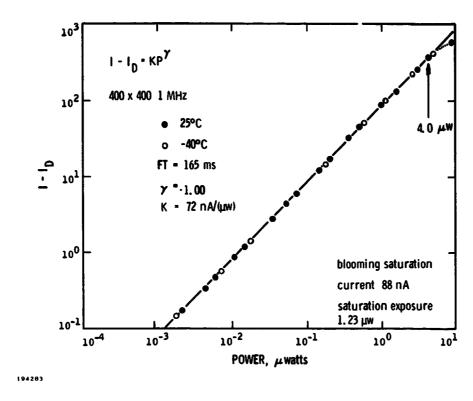


Figure 6-17. Signal I - ID Versus Incident 2854° Radiation for 24°C and -40°C

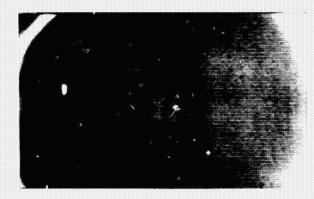
The temperature dependence of the curve showing CCD response versus incident light level is shown in Figure 6-18 for a 400 X 400 CCD. There is essentially no dependence of signal current as temperature for a given power input using a 2854°K source of radiation.

As indicated by the data in this figure, the saturation power (determined by the onset of blooming) is $1.23 \,\mu\text{W}$ for the 163 millisecond frame time. From this number the saturation exposure is $E_{\text{sat}} = (P_{\text{sat}} \, \tau_{\text{f}})/A$ where A is the device area and $E_{\text{sat}} = 2430 \,\mu\text{J/meter}^2$. Note that the break in the gamma curve occurs about a factor of two above the blooming point. The saturation charge is given by $q_{\text{sat}} = (I_{\text{sat}} \, \tau_{\text{f}})/q$ N where N is the pixel number giving $q_{\text{sat}} = 5.6 \,\text{X} \, 10^5$ electrons. These numbers are representative of the arrays developed. Some arrays were operated at lower clocks; the result was lower values of saturation charge (JPL 11). For a dynamic noise level of 100 electrons which seems a representative noise, the noise-equivalent exposure is $0.43 \,\mu\text{J/meter}^2$.

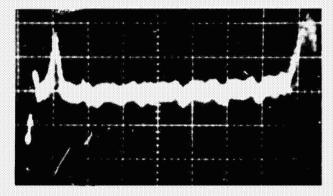
D. UNIFORMITY OF RESPONSE

Several factors affect CCD uniformity. Early devices were affected by the line pairing effect discussed above. This has been eliminated. The next most important mechanism appears to result from membrane nonuniformities, particularly at the edge of the thinning window where the thin-to-thick silicon transistor occurs. The solution to the latter problem is to allow the thinning window to extend well outside the active array area. An alternate approach is to use other etch techniques to provide a sharp thick/thin transition. This is actively being pursued in the follow on to the JPL program. The uniformity of response is also affected by the uniformity of the





RESPONSE TO 0.40 MICRON LIGHT



VIDEO LINE NO. 10 SHOWING OPTIMUM RESPONSE AMPLITUDE

Figure 6-18. Video Response From a Nonuniformly Thinned Array Showing Rings of Optimum Response



proprietary backside thinning process used by Texas Instruments. Nonuniformities in response are often concentric, following approximately the contours of the thinning window on the 100 X 160. Possibly the haze which is often left after thinning is related in some way to the backside accumulation enhancement resulting in patterns such as shown in Figure 6-18. It is, howeve, rather difficult to predict the uniformity of a given device and there is also some variability from device to device. The uniformity as defined in Section V varies around 10 to 15 percent, including blemished pixels. The best 160 X 100's have a uniformity of better than 5 percent using the standard thinning techniques. It appears that the 400 X 400's have ~15 percent response uniformity.

The above comments have addressed the problem of variations in responsivity across an array. Light, localized blemishes also affect the uniformity of array response. At the present time, the best 160 X 100 arrays have no localized defects. However, the 400 X 400's have 10 times the area of silicon and present technology is not eliminating all defects. The exact nature of the defects has not been definitely identified (Section III) but eventually will, we believe, be related to the residual impurity concentration and/or defect concentration in the silicon. To achieve a defect-free device in the sense of the present 100 X 160 arrays shown in Figure 6-10 will require further development work.

In some instances a localized, light blemish will appear only when the device is illuminated. This could result from a small region which is more efficiently accumulated or perhaps from a region which had thinned locally to a greater extent. Such defects are, however, not generally observed. Of course, the uniformity of response as measured by the number of pixels with response sufficiently far from the mean level can, of course, be influenced by the amount of streaking as indicated in Subsection VI.A (Figure 6-3).

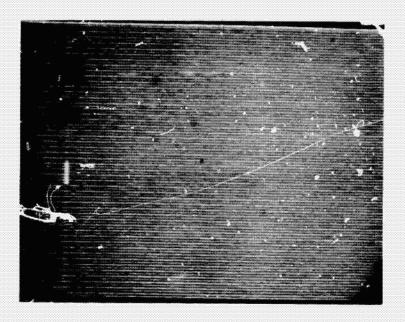
In Figure 6-19 the uniformity of a 100 X 160 array is shown for broadband 3400°K illumination at 24°C and -40°C. Well population corresponds to about 50 percent of a full well.

The uniformity of dark current was affected by amplifier heating effects in early area arrays. This is avoided in later devices (JPL 10) by higher follower load resistors. The magnitude of the numbers given in the Appendixes for uniformity are rather suspect because of the difficulty of accurately defining the video voltage on the MCA corresponding to 4 percent of full well and also to an empty well. Refinements in electronics are required to improve the accuracy of these measurements. Visual inspection of video output on the oscilloscope show pixel-to-pixel variations of about ± 5 percent at 50 percent full well. However, in the most recent arrays, the magnitude of the dark current is so low at -40° C that in the specified exposure time, the dark charge is well below the 4 percent level.

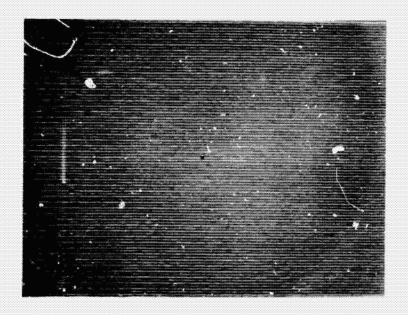
E. SQUARE WAVE AMPLITUDE RESPONSE

As indicated in Section II, resolution capability of the imagers at the Nyquist frequency is 21.9 line power per mm. SWAR taken at 24°C and -40°C are compared in Figure 6-20 and there is essentially no change over this temperature range. Data taken on a 400 X 400 at 24°C is shown in Figure 6-21. Results for the bars parallel to the serial register is sensitive to parallel CTE (circles in Figure 6-21) while bars perpendicular are sensitive to serial register CTE. There appears to be a small decrease in SWAR at Nyquist for the pixel farthest from the output. This data was taken at -39.5°C and the SWAR differences are probably within experimental error. More reliable data taken on JPL II indicates SWAP about 15 percent lower for bars parallel to the serial register at the Nyquist frequency.





A. 4000Å RADIATION



B. 3400°K RADIATION

Figure 6-19. Video Uniformity of Response at 25°C for a 100 X 160



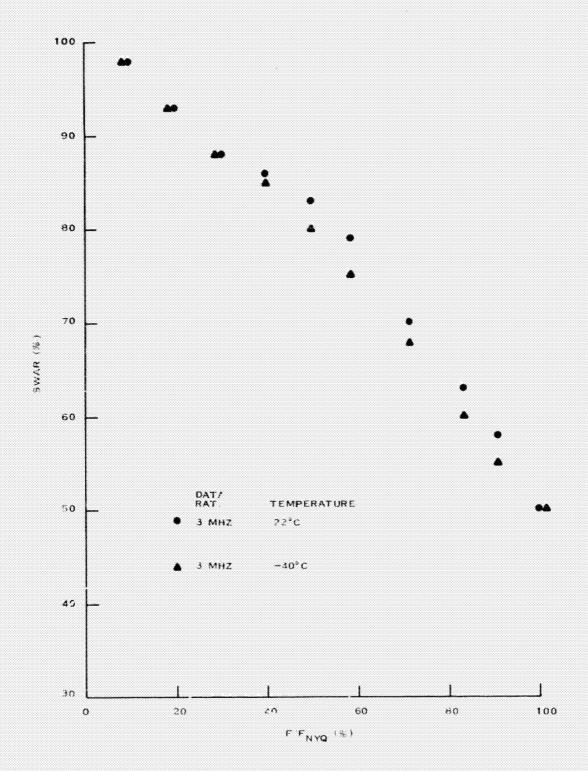
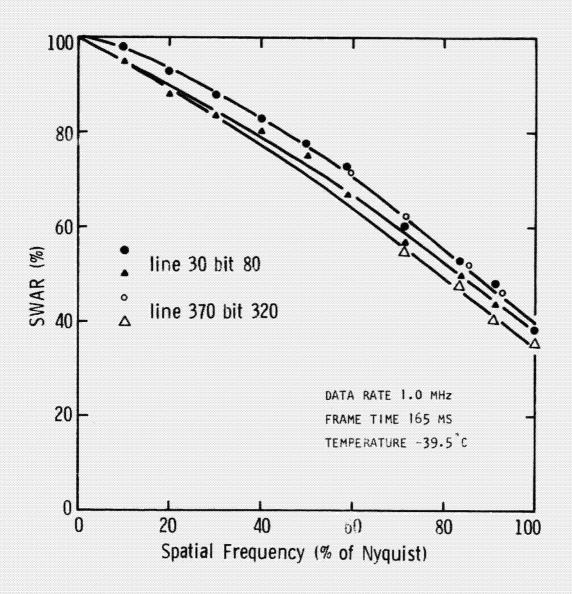


Figure 6-20. SWAR at 24°C and -40°C Showing Essentially No Difference





- BARS PARALLEL TO SERIAL REGISTER
- △ BARS PERPENDICULAR TO SERIAL REGISTER

Figure 6-21. SWAR of a 400 X 400 Array for Pixel Near the Output and Far From the Output



Several factors degrade SWAR at Nyquist from the value expected from the array. These were discussed in Subsection V.J. The main contributions are from: lens MTF, array CTE and from diffusion of photogenerated carriers from the backside of the array. The direct transfer MTF is given by exp $(-N\varepsilon)$ at the Nyquist frequency relative to unity at zero spatial frequency. Here N is the number of charge transfers made by a packet and ε is the losss per transfer. At a point furthest from the output of the 400 X 400, N = 2400 so that for $\Sigma = 1 \times 10^{-4}$ (CTE = 0.9999), the response is down by exp (-0.24) = 0.79. If $\Sigma = 2.10^{-5}$ (CTE = 0.99995), the response is only down to 0.97 at Nyquist. The effects of CTE loss will appear in degradation of SWAR across the array. In a buried-channel array no such dependence is observed for either bars horizontal or vertical with respect to the array. In these measurements the effective number of transfers is 1200 so that the experimental accuracy (of ±5 percent) of the SWAR indicates a CTE of about 0.99992-0.99995 in agreement with experimental measurements injecting a pulse into the serial register.

Surface channel devices have lower CTE than buried channel arrays. Figure 6-22 shows the video output obtained from two 400 X 400 array from the first processed lot of devices. The devices were processed as surface channel to allow initial evaluation of the 400 X 400 design itself. The imagery is excellent but the resolution is not as good as shown earlier in Figure 6-1, due to the lower CTE of 0.999. It is interesting to note that the defect density is quite low for these two devices—comparable with the best buried-channel devices.

Additional SWAR degradation results from the diffusion contribution. This effect depends on the thickness of the membrane and becomes more important as this thickness increases as can be seen from the Crowell Labuda formula in the limit of long minority carrier lifetime and low surface recombination velocity, ¹⁹

viz
$$\approx [\cosh(2\pi f | \mathbf{L}_n)]^{-1}$$

Here f is the bar chart frequency and L_{η} the neutral silicon thickness from the backside to the collecting depletion region. Thus, the expected response depends on membrane thickness, and since $L_{n} \approx 5 \, \mu \text{m}$, variations of 10 percent in thickness at the Nyquist frequency result in about a 5 percent variation in response. It is possible that the CTE loss and diffusion effects offset so that the SWAR appears invariant across an array which gets thinner far from the output, but this is not really consistent with the many observations made.

The data shown in the Appendixes is uncorrected for lens MTF effects. Such corrections are difficult to make accurately, as indicated in Section V. Correction by the factor of 0.65 given in Section II would increase the SWAR at Nyquist for the 400 X 400 arrays from \sim 40 to \sim 60 percent and of the best 160 X 100 arrays from 52 to 80 percent. Unity SWAR is not expected at the Nyquist frequency due to the discrete sampling format of the CCD. This leads to an MTF decreasing as

$$\operatorname{Sin} \frac{\pi f}{f_m} \int \pi f/f_m$$

which = 0.64. Here $f_{\rm m}$ = 2 times the Nyquist frequency. This corresponds to a SWAR degredation of \approx 0.82. Thus, the measurements for the smaller arrays are in satisfactory agreement without invoking any additional degradation. However, the above argument applied to the 400 X 400 will give an expected SWAR (0.82) which is higher than the corrected







Figure 6-22. Imagery With Surface Channel (CTE 0.999) 400 X 400 CCDs (Compare Figure 6-1)



experimental value (0.60). It is expected that the diffusion contribution will be the same for the two arrays and the lack of dependence of the data on position in the array suggest very little CTE degradation. The discrepancy is not resolved fully at this time and detailed corrections for the system must be obtained in future studies if the individual components are to be reliably isolated.

F. DYNAMIC NOISE

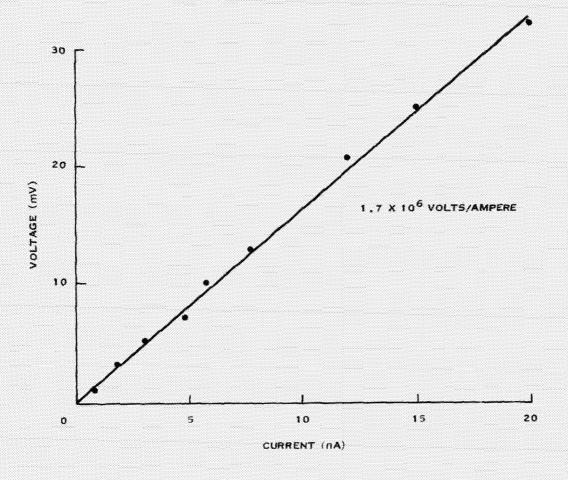
The measurements made to determine the dynamic noise on a CCD output is described in Section V. The data were taken by sampling a single pixel from the center of the array which was read out at 1 MHz. By sampling a single pixel, the noise associated with variations in dark current across the array, i.e., the spatial noise, is eliminated. The MCA samples the output of the video chain, one each frame. For the 100 X 160, this sample time is 16 milliseconds and for the 400 X 400 is 160 milliseconds. Typically, several hundred samples were taken to determine the mean video output and width of the distribution. A resistor network was used to provide a "zero" noise figure and was placed on a ceramic header in the same position of the CCD immediately after the measurement. For the 100 X 160, a dc bias was applied to the gate of the sampling MOSFET and a precharge output waveform used. Noise levels for the 100 X 160 were consistently in the 100 to 150 electron range. An example of the amplifier calibration linearity relating an injected current to an output video voltage, which is necessary to calculate the noise electrons from the observed width of the video voltage, is shown in Figure 6-23. Also shown is the MCA output to indicate the near Gaussian shape of the noise signal. The initial 400 X 400 (JPL 9) indicated a measured noise of 1,300 electrons which almost certainly was due to electronic noise in the measuring circuit, (JPL measured 70 electrons on this device after delivery.) The noise from the JPL 11 was 320 electrons as shown in the appendixes. Generally, noise was higher in the 400 X 400's than from the 100 X 160's. There seems to be no intrinsic reason why this should be the case. In order to determine that the video output from the CSH amplifier was giving a true indication of CCD noise, optical input was made to the device. For n electrons per pixel, a noise of n'2 should be observed at sufficiently high light levels that the intrinsic noise was much less than n^{1/2}. It was consistently observed that the measured noise would be very close to the shot noise values at full well defined by blooming and that, for further increase in optical input, would drop very rapidly. This point could be taken as a measure of full well and always occurred at about 0.5 of the light level at which the gamma curve breaks from unity slope.

The question arises as to the source of the noise level measured in the CCD arrays. There are several noise sources which contribute. The most important in the present experiments is probably output amplifier noise. The technique of correlated double sampling²⁰ provides an off-chip detection scheme which is linear, stable, and requires only a few MOSFETs. The final output is in sample-and-hold format, which allows high-gain amplification. However, care is required in timing the clamp-and-sample pulses and in the appropriate filtering.

The circuit used to implement this technique has already been given (Figure 5-1). The noise due to preset, resulting from thermal noise in the reset switch channel (S_1) , is

$$n = \frac{1}{q} (kTC)^{t_2} \sim 200 \text{ electrons}$$
 (6-1)





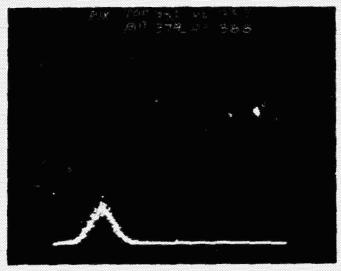


Figure 6-23. Calibration of Noise Amplifier Chain To Relate Current to Voltage for the CCD and Shape of Noise Signal From Output From MCA Display



for an output node capacitance of 0.25 pF. A further discussion, following the text of a recent review article²¹ describing detailed noise studies at Texas Instruments on 150 X 1 linear, buried-channel CCDs is presented below.

The CDS technique provides an approach for removal of this preset noise. As discussed by White, et al., when the preset switch is opened, node A has a time constant given by $R_{\rm off}$ $C_{\rm o}$ where $R_{\rm off}$ is the resistance to ac ground of node I when transistor SI is off and is typically >10¹⁰ ohms. The preset noise, n_1 , will therefore be correlated between any two samples which are taken after the preset at t_1 . The output is taken to be the difference in voltage of the samples at times t_2 and t_4 (shown in Figure 5-2) subject to the constraints $t_1 < t_2 < t_3 < t_4 < t_5$. In this case, the preset noise will approximately cancel and only the change in voltage due to the transfer of the signal charge will be observed. If the time between the two samples $(t_4 - t_2)$ is too long compared to the time constant $R_{\rm off}$ $C_{\rm o}$, the correlation of the noise is decreased and the noise level, n_A , will be measured

$$n_{A} = n_{1} \left[2 \left(1 - e^{-\frac{(t_{4} - t_{2})}{R_{OFF} C_{O}}} \right]^{\frac{1}{2}} \right]$$
 (6-2)

where n_1 which is given by Equation (6-1) is the preset noise without CDS. The effective value of $R_{\rm off}$ which was observed was on the order of 10^8 ohms, which required the interval t_4-t_2 to be less than $5\,\mu s$ for suppression of the preset noise. The reason for this low value of $R_{\rm off}$ is thought to be due to surface leakage. Therefore, if very low-frequency operation is desired, care should be taken to reduce this leakage.

If the interval $t_4 - t_2$ is much greater than $R_{\rm off}$ C_o , the preset noise will actually be increased by the use of CDS. This increase occurs because the noise voltage sampled at the times t_2 and t_4 are then totally uncorrelated and when the difference in voltage is taken between these two samples, the noise, n_1 , from each sample adds in quadrature and yields a resultant noise level of $\sqrt{2} \, n_1$ which can be seen from Equation (6-2).

The circuit which was used to take the difference in the two samples is shown in Figure 5-1. The signal was capacitively coupled by capacitor C_c and then clamped to a dc voltage at time t_2 . The voltage difference was sampled and held on capacitor C_{SH} by briefly closing MOSFET switch T_s at time t_4 . The buffer amplifiers A2 and A3 were both MOSFET source follower circuits.

1. Noise of Clamp-and-Sample Circuits

In this and the following sections expressions will be obtained and evaluated for the various noise sources which contribute to the total output noise and they will be evaluated and compared with the measured results on 150 X 1 linear CCD registers.

The clamping of capacitor C_c and the sampling by S3 which sets C_{SH} are subject to the same considerations applied to the preset of node l [Equation (6-1)] with respect to the uncertainty of voltage on capacitors C_c and C_{SH} except there is no suppression by the double sampling. Therefore, the equivalent number of rms noise electrons referred to the CCD channel, n_D , resulting from the clamping operation at time t_2 is given by,



$$n_D = \frac{1}{q} \frac{C_o}{G_1} \left(\frac{kT}{C_c} \right) \approx \frac{400 \text{ e}^-}{G_1} C_o (Pf) C_c (pf)^{-\frac{14}{2}}$$
 (6-3)

in which G_1 is the gain of MOSFET amplifier A1. A similar expression can be obtained for noise due to the sample and hold,

$$n_E = \frac{1}{q} \frac{C_o}{G_1 G_2} \left(\frac{kT}{C_{SH}}\right)^{\frac{1}{2}} \approx \frac{400 \text{ e}^-}{G_1 G_2} C_o (Pf) C_{SH} (pf)^{-\frac{1}{2}}$$
 (6-4)

in which G₂ is the gain of amplifier A2.

Choosing suitably large values of C_c and C_{SH} will result in a negligible contribution of noise from the clamp-and-sample operations. For the circuit which was actually implemented the calculated noise levels from these sources are $n_D = 7$ e and $n_F = 9$ e.

The noise contributed by the buffer source follower amplifiers A2 and A3 can also be made acceptably small by proper choice of components. In the realization used in these measurements standard n-channel MOSFETs were used which had a low white noise (thermal noise) component but unfortunately had a rather high 1/f noise which was characterized by a corner frequency near 100 kHz. An increase in the output noise at low frequencies was observed due to this excess noise but it was not sufficiently large to significantly degrade the subsequent measurements of other noise sources.

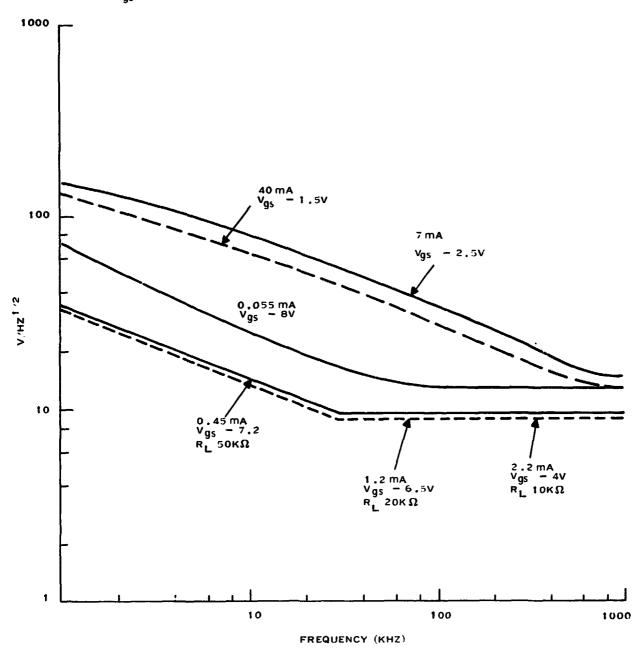
2. 1/f Noise of Source Follower, A1

The rms noise contributed by the amplifiers A2 and A3 is unaffected by the CDS operation; however, the noise generated by on chip amplifier Al is substantially modified because the noise is generated before the CDS circuit. One effect on the noise of A1 which was pointed out by White, et al. is that noise at frequencies that are much less than $(t_4 - t_2)^{-1}$ is substantially suppressed. This characteristic of CDS is especially effective in suppressing the 1/f noise of Al as long as the 1/f corner frequency of Al is sufficiently low. If, on the other hand, the 1/f noise corner is significantly greater than $(t_4 - t_2)^{-1}$, excess noise will be measured at the output. Since 1/f noise in MOSFETs is believed to be due to trapping in surface states, substantial reduction in 1/f noise can be obtained if these transistors are operated in a buried-channel mode (i.e., the signal is away from the Si-SiO₂ interface). Figure 6-24 shows noise measurements on a MOSFET for various values of drain current. At low In the follower is acting as a buried-channel device while at higher currents the charge interacts with the surface and the noise increases. Note the increasing noise at lower frequencies. This data also shows that use of higher load resistances (50 kilohm) to limit power dissipation on chip do not increase noise. To fabricate a buried channel transistor it is only necessary to implant the MOSFET with the same dose which was used to make the buried channel CCDs and to then operate at sufficiently low current levels to keep the conducting channel buried.

For reasons which will be discussed below, the time interval $(t_4 - t_2)^{-1}$ should be set to $2 f_c$, so that for clock rates greater than 25 kHz substantial suppression of the 1/f noise will occur for a buried channel MOSFET, while a large amount of excess noise will be introduced at the lower clock rates if a surface channel MOSFET were used.



 $\rm R_{L}$ is the Load resistor $\rm v_{\rm QS}$ is the source gate voltage



194290

Figure 6-24. Noise Measured on an Isolated MOSFET With Different Drawn Currents, ID



3. Thermal Noise of Source Follower, A1

Besides suppressing the 1/f noise of transistor A1, the CDS circuit also affects the white (thermal) noise component generated by this device. Unfortunately, the effect of CDS is to increase the contribution from this source instead of suppressing it. In fact, it will be shown that this noise component is the dominant source of noise in the entire output amplifier. The optimization of timing and band limiting, which was referred to in the introduction and which will now be discussed, is an attempt to decrease the contribution of noise from this one source.

The purpose of the single pole low pass filter with time constant R_1C_1 which follows A1 in Figure 5-1 is to band limit the thermal noise of transistor A1 and thus to reduce its contribution to the rms noise. The effect of this bandlimiting is to introduce correlation of this noise between the two samples at t_2 and t_4 . Taking this correlation into account, the resultant rms noise after band limiting and double sampling is given by

$$n_{B} = \frac{C_{o}\sqrt{V_{T_{2}}}}{q G_{1}} \left(\frac{1}{4 R_{1} C_{1}}\right)^{\frac{1}{2}} \left[2\left(1 - e^{-\frac{(t - t_{2})}{R_{1} C_{1}}}\right)\right]^{\frac{1}{2}}$$
(6-5)

in which $\sqrt{V_{T}}$, is given by 16

$$V_{T_1} = G_1 \left[4kT \left(\frac{3}{2} g_m + \frac{1}{R_L} \right)^{-1} \right]^{\frac{1}{2}}$$
 (6-6)

where $G_1 = g_m R_L/(1 + g_m R_L)$, R_L is the load resistor of the source follower and g_m is the transconductance of the MOSFET A1. From Equation (6-5) it can be seen that either decreeasing the bandwidth of the R_1C_1 filter (increasing the band limiting of the wide band noise $\sqrt{T_2}$) or decreasing the ratio $(t_4 - t_2/R_1C_1)$, (increasing the correlation between the two samples), will result in a decreased noise level. Therefore, it would appear desirable to increase R_1C_1 while decreasing the time between the clamp and sample pulses. However, as the time constant R_1C_1 of the filter is increased the voltage swing which represents the signal is attenuated by the factor,

$$[1 - e^{-(t_4 - t_3)}/R_1C_1]$$

To maximize this factor the largest possible amount of time should be given for the signal transient to occur. Therefore, the sample at t_4 should occur just before the following preset occurs at t_5 .

Another consideration which also limits the maximum size of R₁C₁ is that a fraction

$$e^{-(t_2-t_1)}/RC$$

of the preset noise, n_A , will remain after the clamp has occurred because of the correlation effects introduced by the bandlimiting. This fraction can be decreased by minimizing the width



of the preset pulse $(t_1 \approx t_0)$ and by clamping (i.e., the sample at t_2) just before the signal is transferred at t_3 . Therefore, the tradeoff involved in choosing the bandwidth of the low pass filter, R_1C_1 , is that the wideband noise of A2 should be bandlimited to as low a frequency as possible which implies a long time constant: however, this long time constant attenuates the signal swing as well as decreases the preset noise suppression.

A suitable compromise of the above considerations is to allow three to four time constants (R_1C_1) between the preset and claim pulses as well as between signal transfer and the sample pulse. The optimum timing subject to this constraint is given by

$$t_1 - t_0 \ll T_c \tag{6-7}$$

$$t_2 - t_0 \approx t_3 - t_0 \approx \frac{t_c}{2}$$
 (6-8)

$$t_4 - t_0 \approx T_c \tag{6-9}$$

and to obtain four time constants for the above mentioned intervals the low pass filter should have a bandwidth, $f_{3 dB} = \frac{1}{2}\pi R_1 C_1$, given by

$$f_{3 dB} \approx \frac{4}{3} f_c \tag{6-10}$$

From Equation (6-9) it is found that with this band limiting and timing sequence that the effect of CDS on the noise voltage, $\sqrt{V_{T_1}}$, [Equation (6-6)] generated a T_2 is to increase the rms level by a factor of $\sqrt{2}$ over the noise level which would be obtained without CDS. This increase in noise is due to the lack of correlation which exists between the clamp and sample pulse because the bandlimiting (which has been optimized taking this effect into account) is too wide to provide correlation between the two samples. The effect is similar to that discussed in Section VI in which the preset noise could also be increased by a factor of $\sqrt{2}$.

Evaluating Equation (6-5) for the rms noise due to the thermal noise of T_2 at a clock rate of 500 kHz, including processing by the CDS circuit (with timing and bandlimiting given in Equations (6-6) through (6-9) yields an rms noise level of $n_B = 21 \, e^-$, which as pointed out previously is the largest noise source in the output amplifier.

Evaluating Equations (6-3), (6-4), and (6-5), and summing the results (in quadrature) results in a total expected output amplifier noise level of $25 e^{-}$.

4. Dark-Current Noise

Other sources of noise come from the storage and transfer of signal charge in the CCD. The two most important sources for a buried-channel device are dark current and bulk state trapping noise.

Since a CCD (buried or surface channel) is operated in deep depletion, there exists a thermal generation of carriers which is attempting to reestablish an equilibrium condition.¹⁵ Electrons generated in this way are collected in the buried channel along with the signal charge.



The variation in the amount of electrons generated and subsequently collected is characterized by shot noise, i.e., the number of rms noise electrons is the square root of the mean value of the collected electrons. For a dark current level of J_D (A/cm²) the number of rms noise electrons, n_{J_D} is given by

$$n_{J_D} = \left(\frac{J_D A_S M}{q f_c}\right)^{V_2}$$
 (6-11)

where A_S is the area of single stage (four gates for a four-phase device) and M is the number of stages.

In general, the dark current was found to be characterized by shot noise; however, for devices in which localized avalanching was occurring (spikes) the noise was sometimes in excess of shot noise. Care was taken to avoid measuring noise on pixels located at or close to dark-current spikes in the imagers.

Bulk state trapping noise has been found in measurements of 150 X 1 registers at Texas Instruments to account for all the remaining noise after the noise due to dark current and the output amplifier have been subtracted in quadrature from experimental measurements. Bulk trapping noise depends on the size of the transferring charge packet and can be investigated in detail by using a very low noise input to the CCD. For several devices tested the rms noise electron level was 20 to 30 electrons measured at 500 kHz. In these devices the density of bulk traps was about 2×10^{12} cm⁻³.

The conclusions are that the measured noise level of about 100 electrons in the CCD imager comes from either the CDS circuitry or the on-chip source follower. While it is possible that bulk states of 10^{13} cm⁻³ would give these levels, this is not a strong possibility because of similar processing on the 150 X 1 and area devices. Further work is required to isolate the noise contributions in the imagers as has been successfully demonstrated for the smaller devices.



SECTION VII CONCLUSIONS

This program has developed large-area CCD imagers with 400 X 400 pixels. Impressive progress has been made since early 1974 when this program began. At that time only 64 X 64 arrays using single-level metalization had been made by Texas Instruments. These devices were surface channel, hence, low CTE and were rather unstable because of gaps in the electrode structure. As a result of this contract, 100 X 160 and 400 X 400 arrays with reduced 0.9 × 0.9 pixel dimensions were fabricated with CTE >0.9999, excellent resolution, extremely low dark current of 1 nA/cm² at 24°C and good uniformity of response. In fact, the 400 X 400 imagery is, in the author's opinion, at least of equal quality to that produced by any other CCD presently fabricated. As clearly indicated by a recent presentation of the 400 X 400 capabilities, the dark current of the Texas Instruments arrays seem generally to be well below that which can be achieved elsewhere.

Several aspects of large CCD arrays require further intensive development. Perhaps the most important in the loss encountered in device processing. Improved techniques need to be developed. Further work is required to increase uniformity of response to optical radiation—this is of considerable importance for system application. This area is the subject of continuing development in a follow-on program to that reported here. The achievement of high responsivity at 4000 Å is a very intriguing result and suggests that further work to understand and control the surface-band bending may result in shorter wavelength response.

The quality of the 400 X 400 arrays suggests an extension to an even larger format -800 X 800. Many options must be considered here and some are discussed in Appendix H. It seems at present that a pixel must be used to maintain a reasonable size silicon chip for each array. This reduction will result in lower dynamic range for the CCD and may impose extreme tolerances of processing the array. These potential problems, however, should be attacked and the requirements for the large array defined clearly.



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for

Customer Jet Propulsion Lab

Contract No. 953788

Device No. JPL 15 (140-7-2)

Device Type 100 X 160 buried channel

CCD OPTICAL AND ELECTRICAL CHARACTERIZATION TEST REPORT

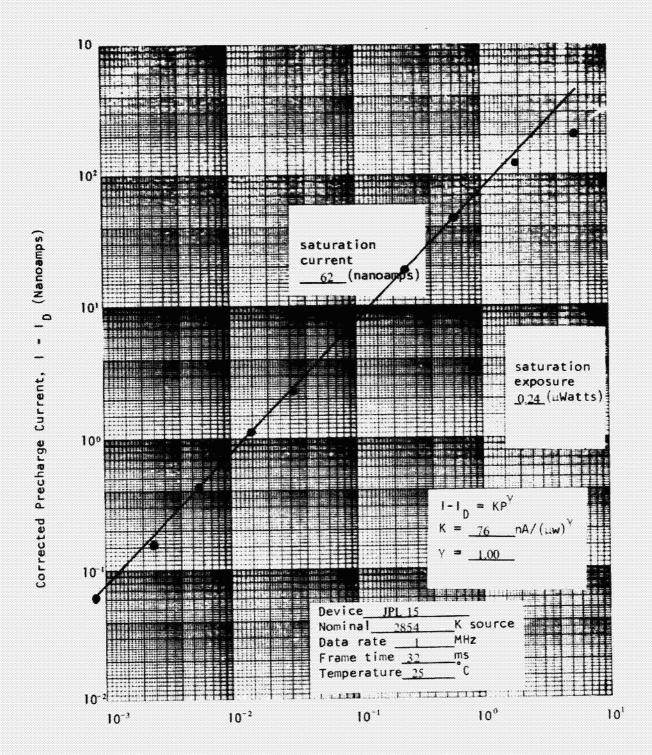
1.	CCD DEVICE NUMBERJPL 15	Date <u>12-1-75</u>
2.	DEVICE TYPE 100 X 160 III buried channel	
	Header type 40 pin DIP	
	Active area 0.0836 cm ² , pixel o	imensions 0.9 mils X 0.9 mils
3.	UPERATING LEVELS in volts	
	SUBS (substrate) -2 V P CLK (parallel clocks 8 V S CLK (serial clocks) 10 V SID (serial input diode) 25 SOG (serial output gate) 2.5 V (precharge pulse amplitude) 18	Vref (precharge reference) 21 V Vref (drain voltage) 27 V Vdd (load bias)
4.	AMPLIFIER CONFIGURATION used for the te Source follower Precharge	sts in this report <u>Surface channel</u>
5.	SPECTRAL RESPONSE	
		crons crons crons.
	Frame readout mode, non shutter frame time 32 ms, temperatur population 80 %.	
	Note that quantum efficiencies are unco	rrected for reflection.
6.	WIDEBAND RESPONSE	
	a) Responsivity is $\frac{76}{\text{from saturation dow}}$ (mi b) γ is $\frac{1.0}{\text{sensitivity is }} \frac{76}{\text{from saturation dow}}$ electrons/p $\frac{100}{\text{mJ/m}^2}$.	n to saturation divided by <u>520</u> .
	d) Numerical integration of spectral r population yields a sensitivity of pared to the directly measured sens microwatt at the same well populati	76 nanoamps/microwatt com- itivity of 76 nanoamps/
	Frame readout mode, non shutter frame time 32 ms, temperat	ed, data rate <u>l</u> MHz, ure <u>25 °C, 2854 °K source.</u>
7.	SATURATION EXPOSURE	
	a) Saturation exposure is 3140 μ J/b) A full well contains 7.75×10^5 elecc) Blooming first occurs DOWN th	m ² , for <u>2854</u> OK source. trons. e channels.
	Saturation exposure measured as illumin amplitude difference is achieved betwee frequency bar chart. Bars oriented per direction of blooming.	n light and dark bars of Nyquist

(continued)
Frame readout mode, non shuttered, data rate 1 MHz, frame time 64 ms, temperature 25 °C.
NCISE
a) Number of RMS noise electrons is 90 . b) Noise equivalent exposure is $0.36 \mu J/m^2$ for a 2854 °K source.
Frame readout mode, data rate 1 MHz, frame time 16 ms, temperature 25 °C, off-chip amplifier bandwidth 2 MHz
DYNAMIC RANGE
Dynamic range is $\underline{8600}$, defined as saturation exposure divided by noise equivalent exposure.
DARK CURRENT
Dark current measured by integration technique is $33\ 10^4$ electrons/pixel/sec (1.02 nanoamps/cm ²) at T = 25 °C, compared to 1.06 nanoamps/cm ² using precharge current measurements.
Dark current measured by integration technique is $\frac{6.7 \times 10}{10}$ electrons/pixel/sec (0.0021 nanoamps/cm ²) at T = $\frac{-40}{10}$ °C.
Frame readout mode, data rate 1.0 MHz at T = 25 °C, 0.010 MHz at T = -40 °C. Frame time variable for integration technique, 32 ms for precharge measurement.
DARK OUTPUT NONUNIFORMITY
Dark output nonuniformity (standard deviation divided by the mean) is 0.19 at T = 25 °C.
Frame readout mode, data rate $\underline{}$ MHz, frame time $\underline{}$ ms
RESPONSE NONUNIFORMITY
Wideband response nonuniformity (standard deviation divided by the mean) is $\underline{7.6\%}$ for a $\underline{2854}$ °K source.
Spectral response nonuniformity is $\underline{10.6\%}$ for a $\underline{0.466}$ micron source, and $\underline{102}$ for a $\underline{1.0}$ micron source.
Frame readout mode, shuttered, data rate 0.010 MHz, exposure time 0.25 sec, temperature 25 °C.
BLEMISH COUNT
Number of illuminated blemishes (pixels with a response less than $\frac{25}{\%}$ or more than $\frac{75}{\%}$ of full well with an average illumination level of 50% full well) is $\frac{291}{}$.

CCD	TEST	REPORT		
DEV	ICE N	JMBER	JPL 15	

13.	(continued)
	Number of dark blemishes (pixels with an unilluminated output of more than 4% of full well) is 540% .
	Frame readout mode, shuttered, data rate <u>0.01</u> MHz, exposure time <u>0.25</u> sec, source <u>2854</u> °K, temperature <u>-40</u> °C.
14.	RESOLUTION
	Uncorrected square wave amplitude response at the Nyquist frequency
	a) for bars perpendicular to the serial register
	49 % at line 5 , bit 10 45 % at line 50 , bit 80 44 % at line 95 , bit 150 .
	b) for bars parallel to the serial register
	43 % at line 5 , bit 10 41 % at line 50 , bit 80 39 % at line 95 , bit 150 .
	Frame readout mode, non shuttered, data rate 1 MHz, frame time 32 ms, temperature 25 °C, 3400 °K source, lens Wollensak aperture F/8, highlight illumination level 40 % full well.
15.	CHARGE TRANSFER EFFICIENCY
	Serial register charge transfer efficiency is 0.9999 for 50 % signal pulse, 0 % fat zero, data rate 1 MHz, temperature 250 °C.
16.	RESIDUAL IMAGE
	Residual image is less than 1% .
	Exposure every other frame, highlight exposure greater than 75% full well, data rate 1 MHz, frame time 16 ms, temperature 25 °C.
17.	MEMBRANE FLATNESS over the active area is
	± 12 microns measured at 25 °C.

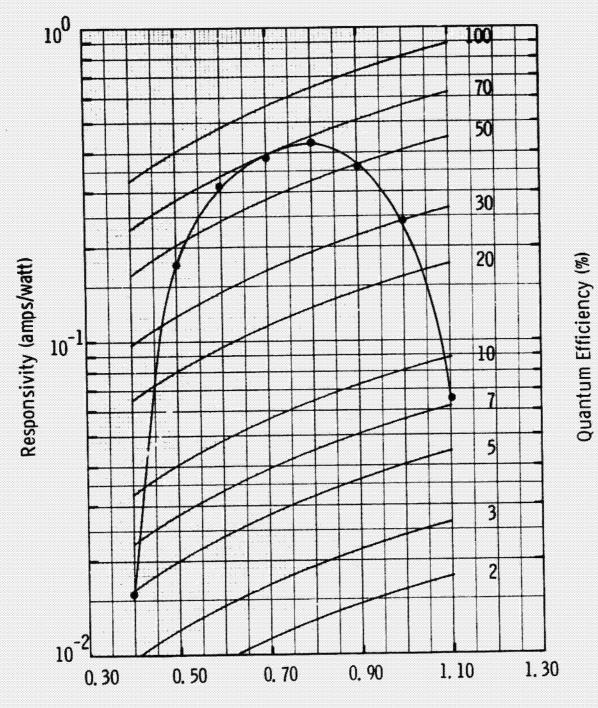
CCD SIGNAL TRANSFER



Incident Power, P (µ Watts)

CCD SPECTRAL RESPONSIVITY

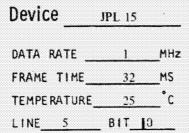
Device JPL-15

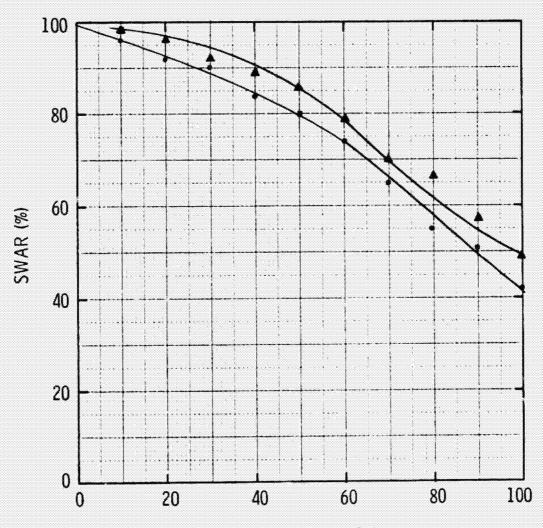


Incident Wavelength (µm)

DATA RATE _____ MHz
FRAME TIME _____ MS
TEMPERATURE _____ °C





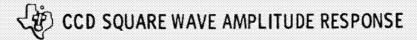


Spatial Frequency (% of Nyquist)

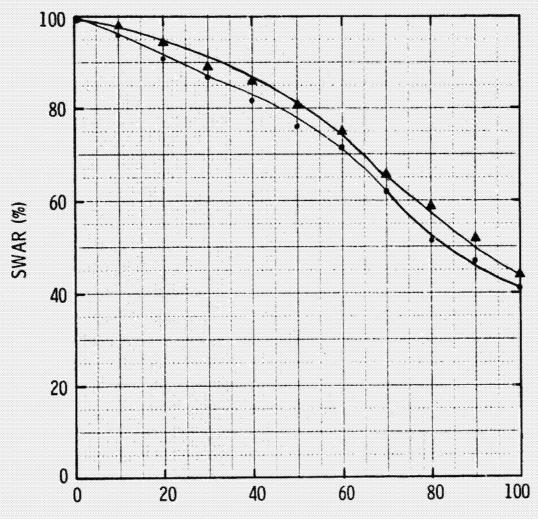
- BARS PARALLEL TO SERIAL REGISTER
- ▲ BARS PERPENDICULAR TO SERIAL REGISTER

3400 K SOURCE MICRON FILTER
LENS Wollensak

APERTURE <u>#/8</u>



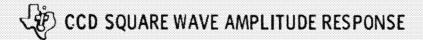
Device	JPL 15	·	
DATA RATE _	1	MHz	
FRAME TIME_	32	MS	
TEMPERATURE	25	*c	
LINE SO	RIT	80	

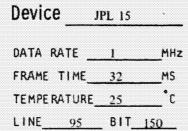


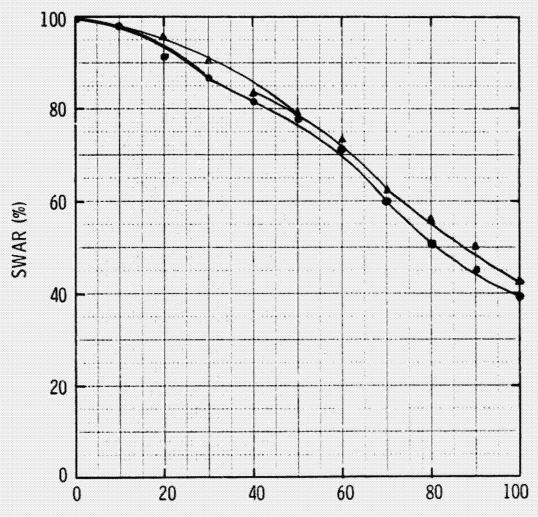
Spatial Frequency (% of Nyquist)

- BARS PARALLEL TO SERIAL REGISTER
- A BARS PERPENDICULAR TO SERIAL REGISTER

34	OO .	K SOUR	ĴE .	N	11 CRON	FILTER
	26.24		***************************************			
LENS	1	×				
~~ · · · · · · · · · · · · · · · · · ·						
APERTL	IRF					
	/ 1 N No.					







Spatial Frequency (% of Nyquist)

- BARS PARALLEL TO SERIAL REGISTER
- ▲ BARS PERPENDICULAR TO SERIAL REGISTER

3400 K SOURCE MICRON FILTER

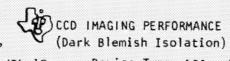
LENS Wollensak

APERTURE f/8

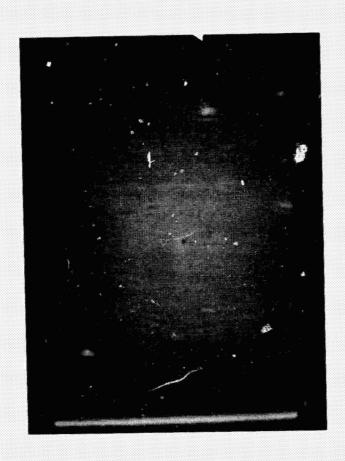


Device Number	JPL 15	D	evice Type	100 x 160	Buried Channel
Light Source	2854	°ĸ	Spectral f	ilter <u> </u>	microns
Temperature	-40	*c	Data rate	0.010	MHz
Frame time	16 x 10 ³	ms			





Device Number	JPL 15	D	evice Type <u>100 x</u>	160 bur	ied channel
Light Source	none	°ĸ	Spectral filter	none	_ microns
Temperature	-40	°c	Data rate	1,0	_ MHz
Frame time	250	ms			

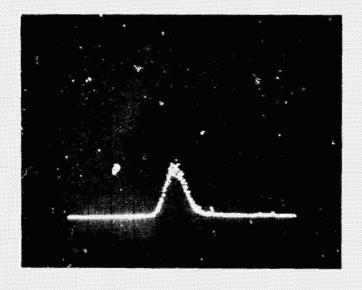


Device Number <u>JPL 15</u> Device Type 100 x 160 Buried Channel



Temperature 25 °C Data rate ____1 MHz Frame time 10⁴ ms

VIDEO MONITOR DISPLAY



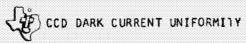
MULTICHANNEL ANALYZER DISM.AY

Average inhibited signal

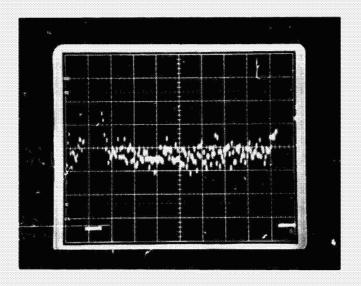
Number of pixels

Average dark signal A-1.2

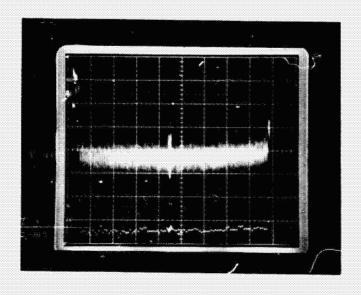
Output level



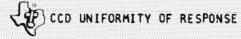
Device Number JPL 15 Device Type 100 x 160 Buried Channel Temperature 24 $^{\circ}$ C Data rate 1 MHz



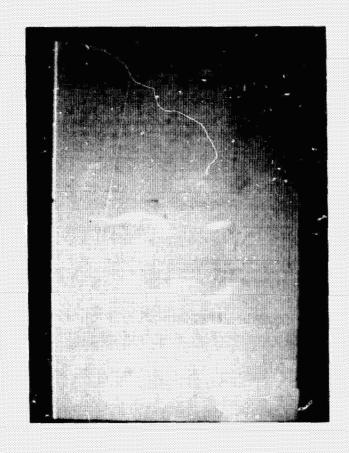
Oscilloscope presentation
Video line number 50



Oscilloscope presentation $\begin{tabular}{ll} \textbf{Complete video frame} \\ & Λ-$1.3 \end{tabular}$



Device Number JPL 15 Device Type 100 x 160 Burled Channel



Light source 2854 $^{\circ}$ K

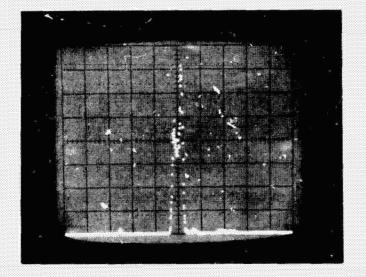
Spectral filter microns

Average well population 50 %Temperature -40 $^{\circ}$ C

Data rate 0.10 MHz

Frame time 16×10^3 ms

VIDEO MONITOR DISPLAY

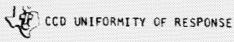


MULTICHANNEL ANALYZER DISPLAY

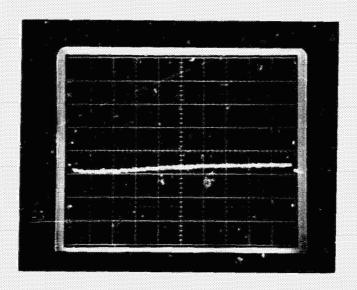
Number of pixels

Average inhibited signal

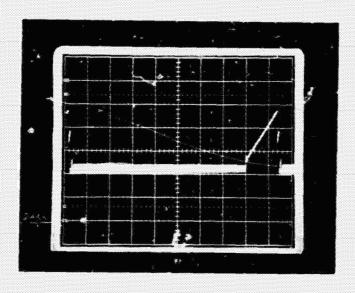
Average response A-14 Output level



Device Number JPL 15 Device Type 100 x 160 Buried Channel Light source 2854 $^{\circ}$ K Spectral filter - microns Average well population 50 % Temperature -40 $^{\circ}$ C Data rate 0.010 MHz Frame time 16×10^3 ms



Oscilloscope presentation Video line number 50



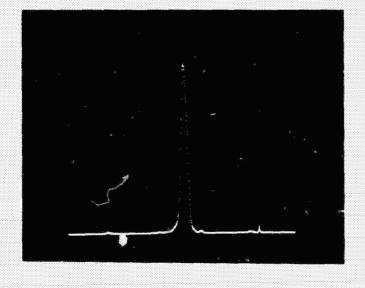
Oscilloscope presentation Complete video frame

Device Number JPL 15 Device Type 100 x 160 buried channel



Light source 2854 Or Spectral filter 0.466 microns Average well population 50 % Temperature -40 OC Data rate 0.010 MHz

VIDEO MONITOR DISPLAY

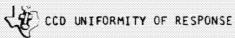


MULTICHANNEL ANALYZER DISPLAY

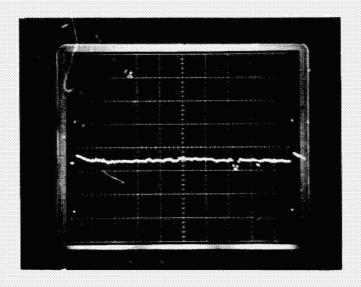
Number of pixels

Average inhibited signal

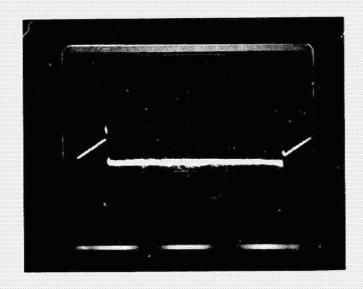
Average response A-16 Output level



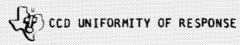
Device Number JPL 15 Device Type 100 x 160 Buried Channel Light source 2854 K Spectral filter 0.466 microns Average well population 50 % Temperature -40 C Data rate 0.010 MHz Frame time 16×10^3 ms



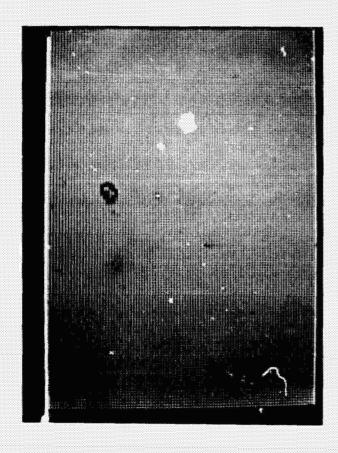
Oscilloscope presentation Video line number <u>50</u>



Oscilloscope presentation Complete video frame



Device Number JPL 15 Device Type 100 x 160 buried channel

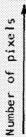


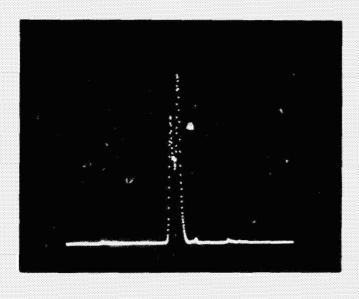
Light source 2854 Ox Spectral filter 0.90 microns

Average well population 50 % CT Temperature -40 OCT Data rate 0.010 MHz

Frame time 16 x 10³ ms

VIDEO MONITOR DISPLAY



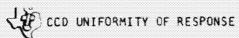


MULTICHANNEL ANALYZER DISPLAY

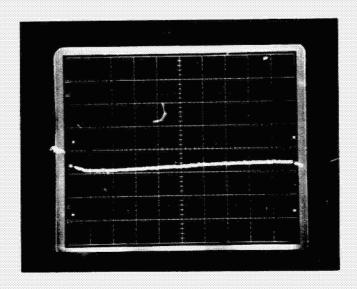
Average inhibited signal

Average response A-18 Output level

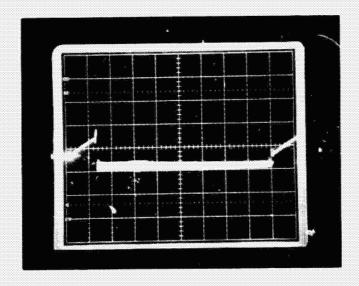
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Device Number JPL 15 Device Type 100×160 buried channel Light source 2854 K Spectral filter 0.90 microns Average well population 50 % Temperature -40 °C Data rate 0.010 MHz Frame time 16×10^3 ms



Oscilloscope presentation Video line number $\underline{50}$



Oscilloscope presentation Complete video frame

TEST AND DEMONSTRATION REPORT JET PROPULSION LABORATORY CONTRACT NO. 953788

1.	CCD DEVICE NUMBER	JPL 3	Date
2.	DEVICE TYPE 16	× 100 conservativ	e design, surface channel
3.	OPERATING LEVELS (olts) unless otherw	rise noted
	PCLK 11	PID	20
	S CLK	PIG	11
	SUBS3	PITG	11
	SID 20		11
	SIG 17	V_D, V_{DD}	
	SOG 4	V _{REF}	
		V _{PC}	
4. ture of	40_ °C unless otherwi	se noted.	5 sec*, a data rate of 0.010 MHz, and a temper- narge current measurements
5.	DARK CURRENT DENS	SITY	
6.		olifier, header and (amps/cm ² connector leakage 1.6 nanoamps/cm ² . % at $\lambda = 0.75$ microns
7.	$\begin{array}{ccc} \text{MINIMUM} & \text{QUANTU} \\ \lambda = & 0.4 & \text{microns} \end{array}$	M EFFICIENCY	Y for the range 0.4 to 1.1 micron is $\underline{0.8}$ % at
8.		ical integration of s	te $2854^\circ K$ source is 42 milliamps/watt at 17 % pectral response, data taken at the same average well population,
9.	GAMMA = 1 ±0.2 from The average gamma =(el down to 0.18 % of saturation which is a ratio of 563 :1.
10.	NOMINAL SATURATION Corresponds to 6.3×10^{-3}		s 0.28 microwatts for a 1.79 sec frame time which
11.	SIGNAL DARK CURRE	NT RATIO is <u>2</u>	8 for a uniform 100 $\mu \mathrm{J/m^2}$ exposure and a frame time of
12.	SIGNAL TO NOISE RA nominal saturation expos		where the number of noise electrons is 1070 at 20 % of
13.	RESPONSE NONUNIFO exposure = ± 18 %.	RMITY for an app	proximate 2854° K source at $\underline{\sim}50$ % of nominal saturation

14.	Number of illuminated blemishes = 2300 at ~ 50 % of nominal saturation exposure.
₹5.	Line residual image < 2 % (V _S - 10).
16.	Uncorrected square wave amplitude response at the Nyquist frequency for an approximate 2854°K source at line $\frac{5 (95)}{5}$, bit $\frac{30 (150)}{5} = \frac{35\% (30\%)}{5}$ for vertical bars, = $\frac{38\% (36\%)}{5}$ for horizontal bars (parallel to the serial register). (V _{SID} = $\frac{10}{5}$
17.	Geometrical paramets
	a) Active area <u>0.124</u> cm ²
	b) Pixel dimensions 1.2 X 1.0 mils
	c) Planarity of thinned surface ± 13.5 microns



JPL 3 DIRECT TRANSFER -40°



JPL 3 TRANSFER AFTER 1.5 MIN STORE -40°



CCD OPTICAL AND ELECTRICAL CHARACTERIZATION TEST REPORT

١.	CCD device number	Date 18 December 1974
2.	Device type 160 X 100 advanced design, buried chan	inel
3.	Geometrical parameters	
	a) Active area <u>0.0836</u> cm ²	
	b) Pixel dimensions 0.9 mils x 0.9 mils	
	c) Planarity of thinned surface is \pm 15	microns
4.	Operating levels in volts (symbols defined o	n page 3) for all tests
	SUBS -1.3 SOG (U) 2	V _{dd}
	P CLK 7 SOG (L) 2	V ₉₉ -22
	S CLK (U) 7 V _{pc} (U) 10	V _{res} 15
	S CLK (L) 7 V _{pc} (L) 10	103
	SID (U) 22 V_{ref} (U) 13	
	5ID (L) <u>22</u> V _{ref} (L) <u>13</u>	
	Amplifier configuration used for the tests i	n this report:
5.	Dark current density is 0.0078 nanoamps/	cm for 0.010 MHz data
	rate, 1.8 X 10 ⁵ millisecond frame time, and	
	measured by integration technique pre	
6.	Peak uncorrected quantum efficiency is	31 % at a wavelength of
	0.72 microns for 0.010 MHz data ra	te, 1.67 × 10 ³ millisecond
	frame time, and temperature of $\frac{-40}{}^{\circ}$ C,	measured by current cali-
	brated on chip amplifier O precharge cur	rent 🛇 .
7.	Minimum uncorrected quantum efficiency over	the range 0.4 to 1.1 microns
	is 0.5 % at a wavelength of 0.40	microns measured the er the
	same conditions as Test 6.	
8.	Wideband responsivity for a <u>2854</u> OK so	urce is <u>46.6</u>
	nanoamps/(microwatt) for a 8 of 1.025	and the wideband sensitiv-
	ity is al nanoamps/microwatt at a we	II population of $\underline{}$ 12 $\underline{}$ %.
	Test performed at <u>0.010</u> MHz data rate,	1.67×10^3 millisecond frame
	time, temperature of $\phantom{aaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaa$	echarge current measurements.

CCD TEST REPORT

8. (cont.) From numerical integration of spectral response data taken at

	the same well population, the wideband sensitivity is 37 nanoamps/microwatt.
9.	A full well contains 1.4×10^6 electrons, defined by the point at which $\chi = 0.8$ for a 0.010 MHz data rate, 1.67×10^3 millisecond frame time and temperature of 40° C. χ is 1 ± 0.2 over a range 150° : 1.
10.	The signal to dark current ratio is 9.6 for a 100 microjoules/m ² exposure of 2854 K radiation and an exposure time of 5×10^3 milliseconds. This exposure corresponds to an incident power of 1.67×10^{-4} microwatts or the creation of 1.22×10^4 electrons per depletion well.
11.	The number of RMS noise electrons is $\underline{400}$ measured at a $\underline{0.100}$ MHz data rate, $\underline{184}$ millisecond frame time and temperature of $\underline{-40}$ °C. The dynamic range is $\underline{3500}$: 1, defined as the number of electrons in a full well divided by the number of RMS noise electrons.
12.	The response nonuniformity (standard deviation divided by the RMS average) is 0.19 at 5 % of full well and 0.14 at 50 % of full well for a 2854 °K source, 0.010 MHz data rate, 6.6×10^3 millisecond frame time and temperature of -40 °C.
13.	Number of illuminated blemishes is 1126 at 5 % of full well and 1406 at 50 % of full well, where blemish pixels are defined as pixels having a response lying outside the mean response by \pm 25 % (same operating conditions as 12).
14.	Dark current nonuni, ormity (standard deviation divided by the RMS average) is 0.96 for a 0.010 MHz data rate, 1.8×10^5 millisecond frame time and a temperature of -40 °C.
15.	Number of dark current blemishes is 1814, where blemish pixels are defined as pixels having a response lying above a factor of 2.0 times the mean dark current (same operating conditions as 14).
16.	Charge transfer efficiency of serial register is 0.9999 for $0.\%$ fat zero, 0.100 MHz data rate, and a temperature of 22

CCD TEST REPORT

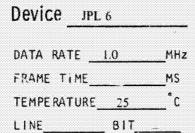
a 289			ude response at the Nyquist frequency for MHz data rate,32 millisecond
			_40 °C and fat zero of 0 %:
SWAR (%)	Line	Bit	
29	15	25	
29	50	80	Bars perpendicular to the scrial register
27	85	145	(Nyquist frequency 21.9 lp/mm)
41	15	25	_
41	50	80	Bars parallel to - the serial register
39	85	145	(Nyquist frequency lp/mm)
	grapiiicai	oata is att	ached to this report.
Definition o			
	of symbols (used in Sect	
Definition of SUBS PCLK		used in Sect e	
SUBS	of symbols i	used in Sect e clocks	
SUBS P CLK	substrate parallel serial c	used in Sect e clocks	
SUBS P CLK S CLK	substrate parallel serial c serial in	used in Sect e clocks locks	
SUBS P CLK S CLK SID SOG	substrate parallel serial conservation serial of serial	used in Sect e clocks locks nput diode	ion 4
SUBS P CLK S CLK SID SOG V PC	substrate parallel serial c serial in serial or precharge	used in Sect e clocks locks nput diode utput gate	ion 4
SUBS P CLK S CLK SID SOG V PC V ref	substrate parallel serial c serial in serial or precharge	used in Sect e clocks locks nput diode utput gate e pulse ampl	ion 4
SUBS P CLK S CLK SID SOG V pc V ref V dd V	substrate parallel serial c serial in serial or precharge	used in Sect e clocks locks nput diode utput gate e pulse ampl e reforence ltage	ion 4
SUBS P CLK S CLK SID SOG V PC V ref V	substrate parallel serial conservation or precharge drain volume	used in Sect e clocks locks nput diode utput gate e pulse ampl e reforence ltage	ion 4

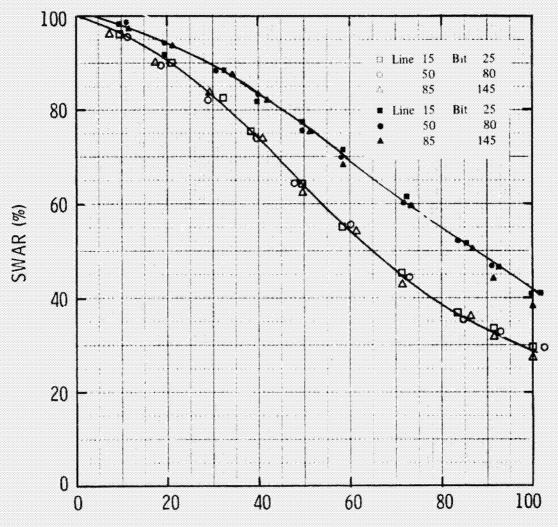
lower

(L)



CCD SQUARE WAVE AMPLITUDE RESPONSE





Spatial Frequency (% of Nyquist)

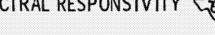
- BARS PARALLEL TO SERIAL REGISTER
- BARS PERPENDICULAR TO SERIAL REGISTER

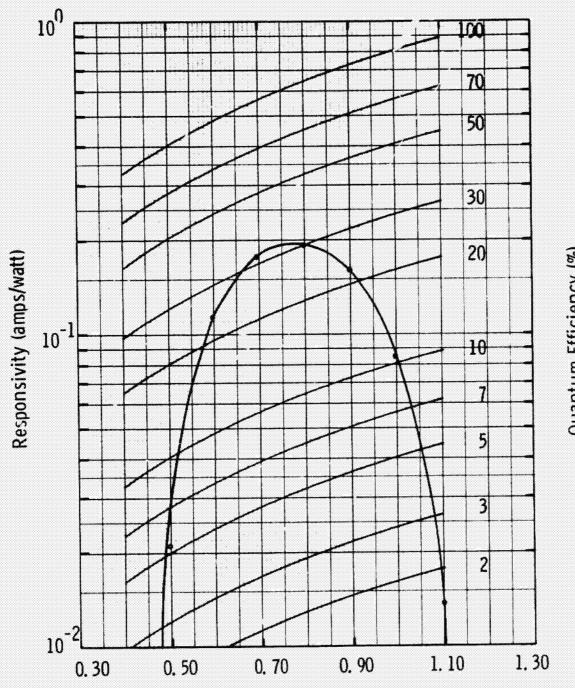
2854 °K SOURCE MICRON FILTER

LENS Wollensak APERTURE

CCD SPECTRAL RESPONSIVITY

Device JPL 6

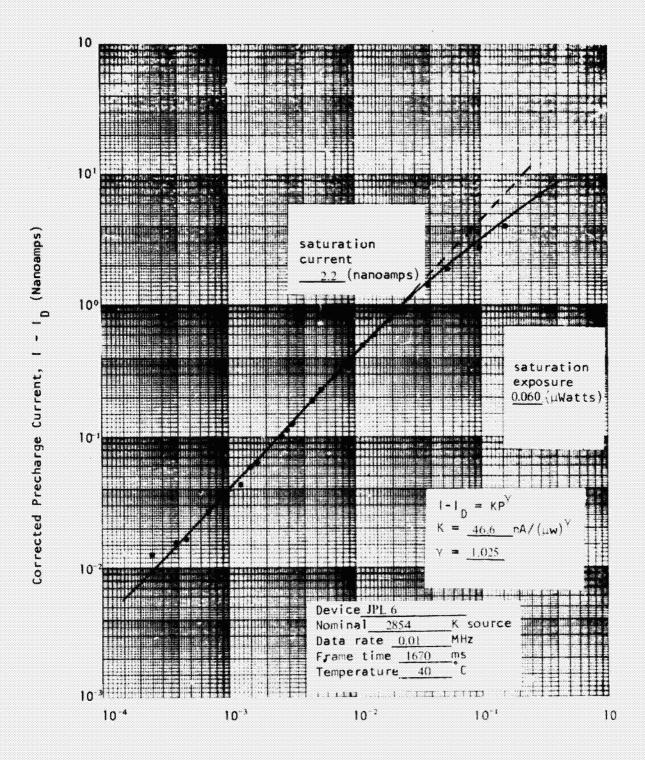




Incident Wavelength (µm)

DATA RATE FRAME TIME $167 \times 10^3 \, \mathrm{MS}$ TEMPERATURE 40 °C B-5

CCD SIGNAL TRANSFER



Incident Power, P (a Watts)

Device Number JPL6 Device Type 160 x 100 Adv. Design, B.C. Light source <u>wideband</u> OK Spectral filter <u>None</u> microns Temperature 22 °C Data rate 1.0 MHz Frame time <u>strobed</u> ms



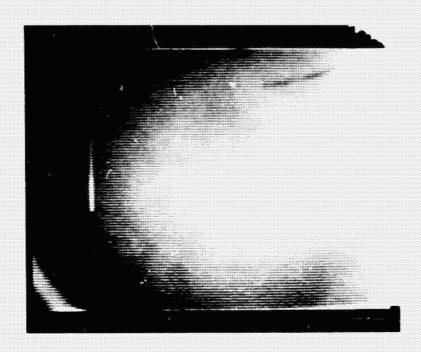
Operating levels in volts

_-1. SUBS P CLK _7.9 S CLK (U) 7.7 S CLK (L)_24___ cip (U) _ 26___ SID (L) _____

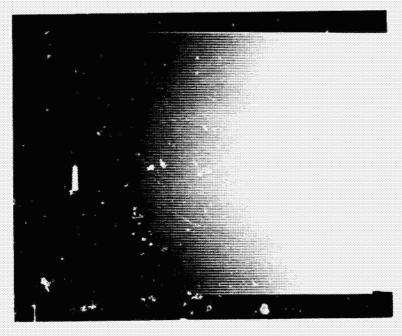
s≎G (U) <u>2.1</u> SCG (L) <u>2.1</u> ν_{ρς} (υ) <u>8.2</u> V_{pc} (L) <u>8.2</u> V_{ref} (U) 13 V_{re}, (L)<u>13</u>

Upper (U) amplifier On-onip sample-and-nold On-onip sample-and-nold

UNIFORMITY OF RESPONSE AS DISPLAYED ON MONITOR (see Sections 12 and 13)



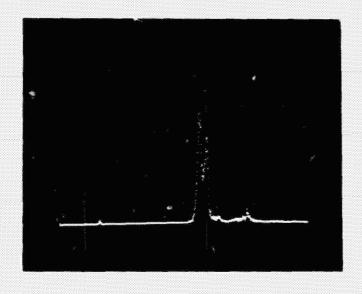
Response of
JPL 6 to
Uniform
Illumination
3 MHz master
Clock 25°C.
Essentially
Unchanged
Except that
blemishes will
disappear at
40° while
remains shading



Dark Current Uniformity JPL 6 3 MHz master clock 25°C Isolated blemishes disappear at 40°C remains shading

UNIFORMITY OF RESPONSE (see Sections 12 and 13) JPL 6 160 x 100

Uniformity of Response 50% full well



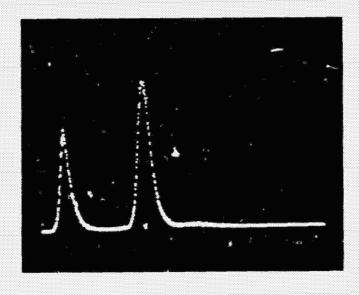
10 KHz Data Rate

Calibration:

no illumination RMS mean response

frame 6.6 sec

Uniformity of Response 5% full well



:: KHz Data Rate

No Illumination RMS mean

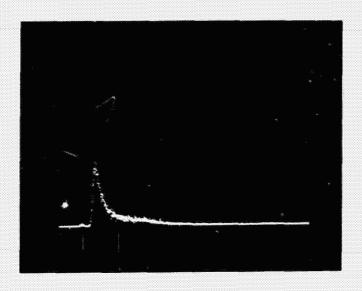
-40°C

frame 6.6 sec

13.4)

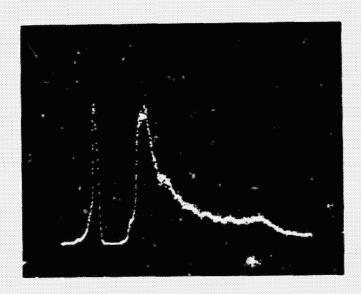
DARK CURRENT UNIFORMITY (see sections 14 and 15) JPL 6 160 x 100

Dark Current Uniformity -40°C 10 KHz



Inhibit RMS Mean Dark Current 180 sec frame time

Dark Current Uniformity 24°C 1 MHz data rate

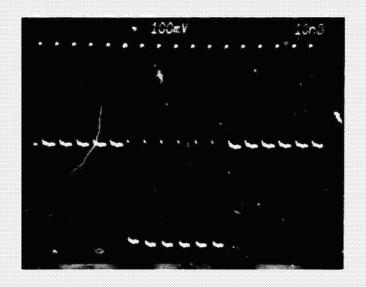


Inhibit

Approx. Mean Dark Current B-10

100 may 100 mg 100 mg

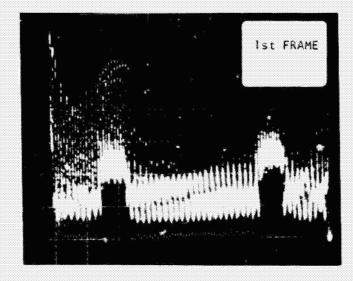
SERIAL REGISTER CHARGE TRANSFER EFFICIENCY (see Section 16) (JPL 6 160×100)



Serial CTE 0.3399

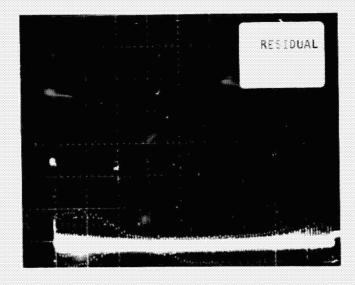
Increased sensitivity at the end of each line

Increase due to light space on bar chart chart between sets of bars

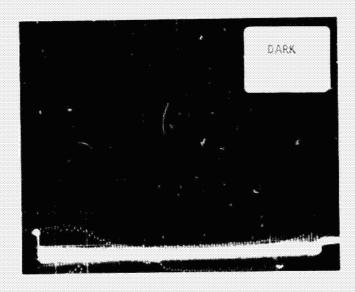


high frequency bar chart (bars 11 to serial) center 50 lines

Residual only appears from pixels which were in near saturation



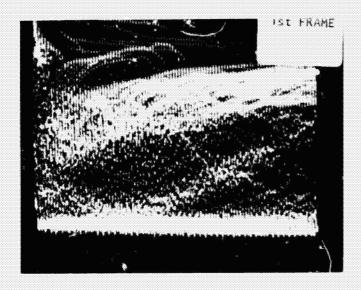
Residual Image Tost

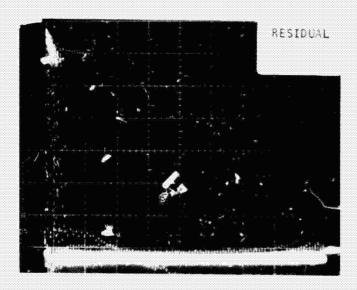


High Frequency Bar Chart (bars $\underline{1}$ to Serial)

Saturation

Residual Image Test





Residual Image on First Few Lines only When First Image is on or very near Saturation $$\rm Be13\ Be14$



CENTRAL RESEARCH LABORATORIES CCD Optical and Electrical Characterization Test Report

for

Customer JET PROPULSION LABORATORY

Contract No. 953788

Device No. JPL 9

Device Type 400 X 400 buried channel

CCD OPTICAL AND ELECTRICAL CHARACTERIZATION TEST REPORT

1.	CCD DIVICE NUMBER JPL 9 Date 22 July 75
2.	DEVICE TYPE 400 X 400 buried channel area array
	Header type 40 pin dual inline
	Active area 0.836 cm ² , pixel dimensions 0.9 mils X 0.9 mils
3.	OPERATING LEVELS in volts
	SUBS (substrate) 0 V_{ref} (precharge reference) 15 P CLK (parallel clocks 8.5 V dd (load bias) 30 S CLK (serial clocks) 10 V dd (load bias) SID (serial input diode) 25 SOG (serial output gate) 2 V_{pc} (precharge pulse amplitude) 16
4.	AMPLIFIER CONFIGURATION used for the tests in this report
	On-chip precharge amplifier, off-chip sample-and-hold amplifier
5.	SPECTRAL RESPONSE
	Quantum efficiency is $\frac{3\%}{60\%}$ at $\frac{0.4}{0.75}$ microns $\frac{60\%}{23\%}$ at $\frac{1.0}{0.75}$ microns.
	Frame readout mode, non shuttered, data rate 1.0 MHz, frame time 165 ms, temperature 25 °C, average well population 39 %.
	Note that quantum efficiencies are uncorrected for reflection.
6.	WIDEBAND RESPONSE
	a) Responsivity is 72 nanoamps/(microwatt) Y b) $\sqrt{18} = 1.00 \pm 0.02$ from saturation down to saturation divided by 520 . c) Sensitivity is 2.3×10^{4} electrons/pixel at an exposure of 100×10^{4} .
	d) Numerical integration of spectral response data at 39 ½ well population yields a sensitivity of 74 nanoamps/microwatt compared to the directly measured sensitivity of 72 nanoamps/microwatt at the same well population.
	Frame readout mode, non-shuttared, data rate 1.0 MHz. frame time 165 ms, temperature 25 °C, 2854 °K source.
7.	SATURATION EXPOSURE
	a) Saturation exposure is $\frac{2430}{5.6}$ $_{\rm H}$ J/m , for $\frac{2854}{5.6}$ $_{\rm W}$ Source. b) A full well contains $\frac{5.6}{5.6}$ X $\frac{10^5}{10^5}$ electrons. c) Brooming first occurs $\frac{10^5}{10^5}$ the channels.
	Saturation exposure measured as illumination level at which maximum amplitude difference is achieved between light and dark bars of Nyquist frequency bar chart. Bars oriented perpendicular to the preferential direction of plooming.

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CCD	TES	TR	EPO	RT				
DEVI	CE	NUM	BER		J	PL.	9	

7.	(continued)
	Frame readout mode, non shuttered, data rate 1.0 MHz, frame time 164 ms, temperature 25 °C.
8.	NOISE
	a) Number of RMS noise electrons is $\frac{1300*}{\text{LJ/m}^2}$ for a $\frac{2854}{\text{VK}}$ source.
	Frame readout mode, data rate 1 MHz, frame time 163 ms, temperature 25°C, off-chip amplifier bandwidth 2 MHz
9.	*Influenced by electronic noise off chip DYNAMIC RANGE*
	Dynamic range is 430 , defined as saturation exposure divided by noise equivalent exposure. *Influenced by electronic noise off chip
o.	DARK CURRENT
	Dark current measured by integration technique is $\frac{2.4 \times 10^5}{\text{electrons/pixel/sec}}$ at T = $\frac{25.7}{\text{c}}$ °C, compared to $\frac{8.5}{\text{nano-amps/cm}^2}$ using precharge current measurements.
	Dark current measured by integration technique is 7.3×10^3 electrons/pixel/sec (_0.19_nanoamps/cm ²) at T =39.6_ "C.
	Frame readout mode, data rate 1.0 MHz at T = 25.7 °C, 0.010 MHz at T = -39.6 °C. Frame time variable for integration technique, 165 ms for precharge measurement.
۱.	DARY OUTPUT NONUNIFORMITY
	Dark output nonuniformity (standard deviation divided by the mean) is 0.43 at T = 25 °C.
	Frame readout mode, data rate 1.0 MHz, frame time 1.2×10 ms
2.	RESPONSE NONUNIFORMITY
	Wideband response nonuniformity (standard deviation divided by the mean) is 0.16 for a 2854 $^{\circ}\text{K}$ source.
	Spectral response nonuniformity is $\frac{0.38}{0.38}$ for a $\frac{0.466}{0.466}$ micron source, and $\frac{0.15}{0.166}$ for a $\frac{0.90}{0.90}$ micron source.
	Frame readout mode, shuttered, data rate 0.0102 MHz, exposure time 0.25 sec, temperature -19.5 °C.
3.	BLEMISH COUNT
	Tumber of illuminated blemishes (pixels with a response less than $\frac{25}{6}$ or more than $\frac{25}{132}$ % of full well with an average illumination level of 50% full well) is $\frac{1322}{1322}$.

	CCD TEST REPORT DEVICE NUMBER
13.	(continued)
	Number of dark blemishes (pixels with an unilluminated output of more than 4 % of full well) is 3.65×10^4 .
	Frame eadout mode, shuttered, data rate 0.0102 MHz, exposure time 0.25 sec, source 2854 $^{\circ}$ K, temperature -39.7 $^{\circ}$ C.
14.	RESOLUTION
	Uncorrected square wave amplitude response at the Nyquist frequency
	a) for bars perpendicular to the serial register
	$\frac{38}{36}$ % at line $\frac{30}{200}$, bit $\frac{80}{200}$ $\frac{36}{36}$ % at line $\frac{370}{370}$, bit $\frac{320}{320}$.
	b) for bars parallel to the serial register
	$\frac{38}{39}$ % at line $\frac{30}{200}$, bit $\frac{80}{200}$ $\frac{39}{39}$ % at line $\frac{370}{370}$, bit $\frac{320}{320}$.
	Frame readout mode, non shuttered, data rate $\begin{array}{ccc} 1.0 & \text{MHz}, \text{ frame time} \\ 165 & \text{ms}, \text{ temperature} & -39.5 & \text{C}, & \text{strobe} & \text{K source}, \text{ lens Wollensak} \\ \hline \text{aperture} & \underline{f/8} & \text{, highlight illumination level} & \underline{75} & \text{% full well.} \\ \end{array}$
15.	CHARGE TRANSFER EFFICIENCY
	Serial register charge transfer efficiency is 0.9998 for 60 % signal pulse, 0 ½ fat zero, data rate 1.0 MHz,

16.

RESIDUAL IMAGE

Residual image is less than $\underline{}$

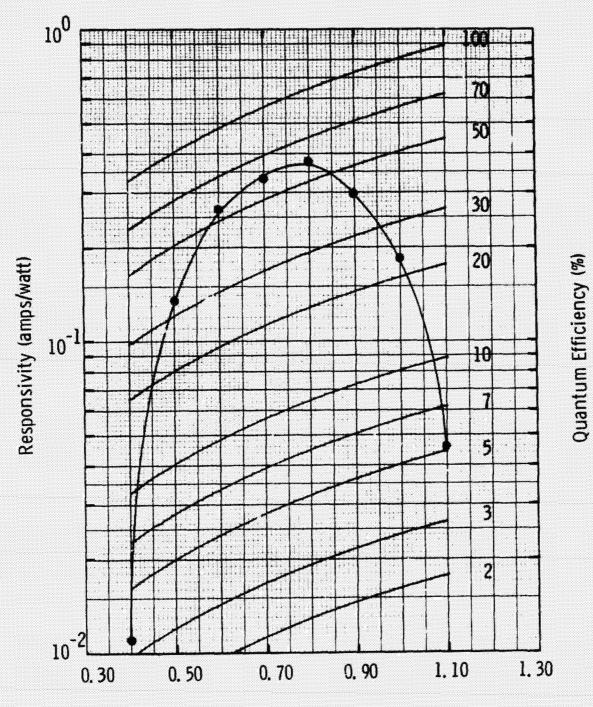
17. MEMBRANE FLATNESS over the active area is

 \pm > 30 microns measured at 24 °C.

Exposure every other frame, highlight exposure greater than 75% full well, data rate 1.0 MHz, frame time 750 ms, temperature -39.5 °C.

CCD SPECTRAL RESPONSIVITY &

Device JPL 9



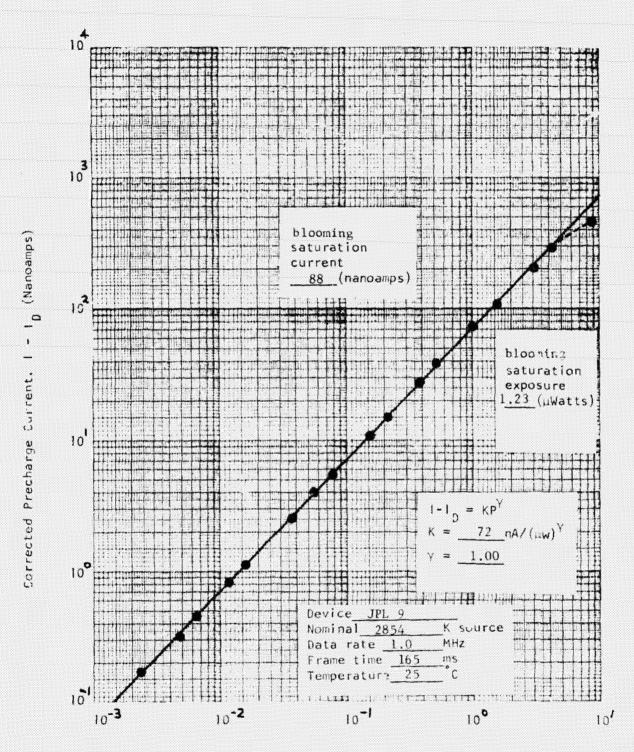
Incident Wavelength (µm)

 DATA RATE
 1.0
 MHz

 FRAME TIME
 165
 MS

 TEMPERATURE
 25
 °C

CCD SIGNAL TRANSFER



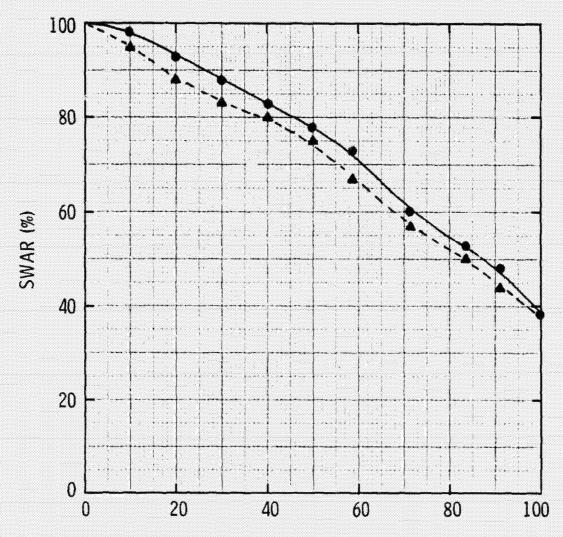
Incident Power, P (µ Watts)



CCD SQUARE WAVE AMPLITUDE RESPONSE

Device JPL 9

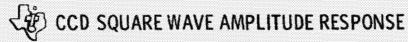
DATA RATE 1.0 MHz FRAME TIME 165 TEMPERATURE -39.5 °C LINE 30 BIT_80



Spatial Frequency (% of Nyquist)

- BARS PARALLEL TO SERIAL REGISTER
- ▲ BARS PERPENDICULAR TO SERIAL REGISTER

Xenon strobe *K SOURCE None MICRON FILTER LENS_ APERTURE



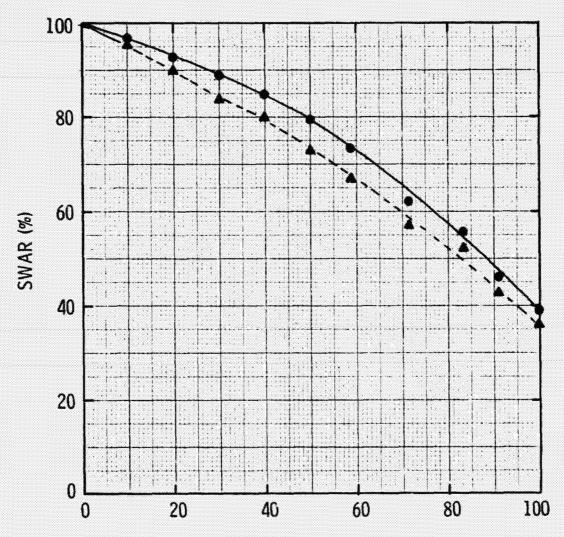
Device JPL 9

DATA RATE 1.0 MHz

FRAME TIME 165 MS

TEMPERATURE -39.5 °C

LINE 200 BIT 200



Spatial Frequency (% of Nyquist)

- BARS PARALLEL TO SERIAL REGISTER
- ▲ BARS PERPENDICULAR TO SERIAL REGISTER

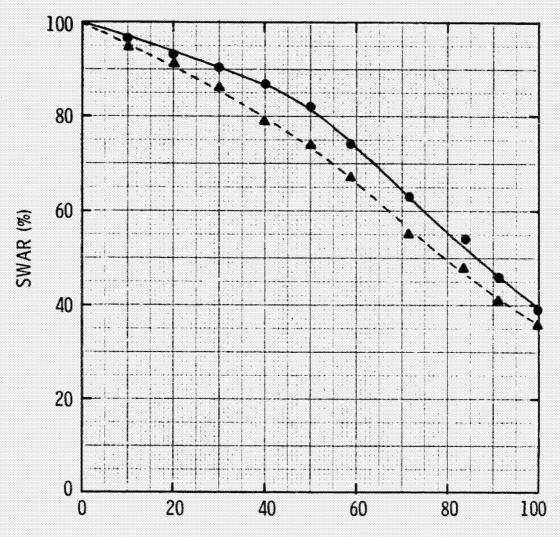
Xenon strobe K SOURCE None MICRON FILTER
LENS_

APERTURE <u>f/8</u>



CCD SQUARE WAVE AMPLITUDE RESPONSE

Device JPL 9 DATA RATE 1.0 FRAME TIME 165 TEMPERATURE -39.5 °C LINE 370 BIT 320

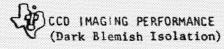


Spatial Frequency (% of Nyquist)

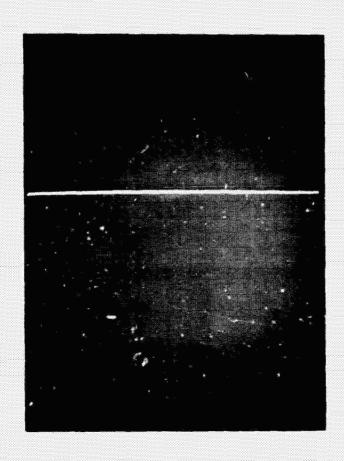
- BARS PARALLEL TO SERIAL REGISTER
- ▲ BARS PERPENDICULAR TO SERIAL REGISTER

Xeno<u>n strobe</u> *K SOURCE None MICRON FILTER LENS

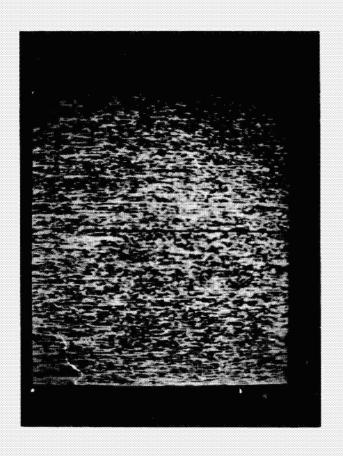
APERTURE



Device Number	JPL 9	Device Type 400 X 4	400 buried channel
Light Source	None	*K Spectral filter _	None microns
Temperature	-39.5	°C Data rate <u>1.0</u>	MHz
Frame time	755	ms	

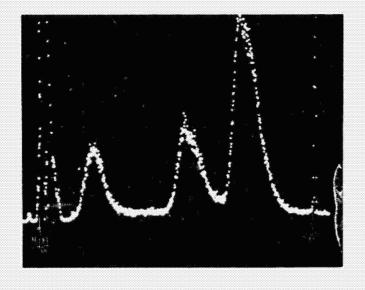


Device Number JPL 9 Device Type 400 X 400 buried channel



Temperature $\underline{26}$ $^{\mathrm{O}}\mathrm{C}$ Data rate 1.0 MHz Frame time $1.2 \times 10^3 \,\mathrm{ms}$

VIDEO MONITOR DISPLAY



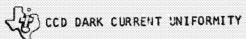
MULTICHANNEL ANALYZER DISPLAY

Average inhibited signal

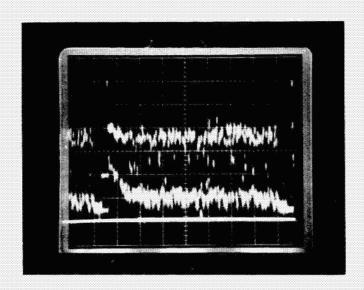
Number of pixels

Average dark signal C-11

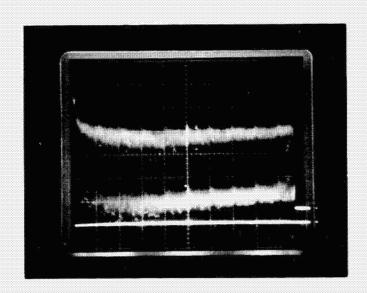
Output level



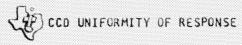
Device Number $\frac{\text{JPL 9}}{\text{C}}$ Davice Type $\frac{400 \text{ X } 400 \text{ buried channel}}{\text{C}}$ Temperature $\frac{26}{\text{C}}$ Data rate $\frac{1.0}{\text{C}}$ MHz



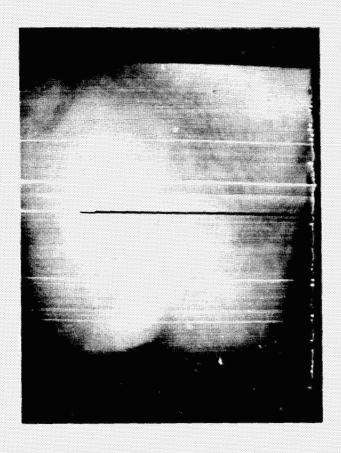
Oscilloscope presentation
Video line number 200



Oscilloscope presentation Complete video frame C-12

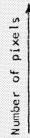


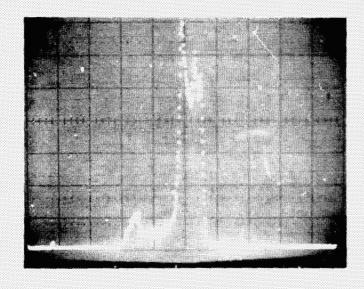
Device Number JPL 9 Device Type 400 X 400 buried channel



Light source 2854 Or Spectral filter 0.90 microns Average well population 50 % Temperature -39.5 OC Data rate 0.010 MHz Frame time 16×10^3 ms Exposure time 250 ms

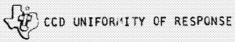
VIDEO MONITOR DISPLAY



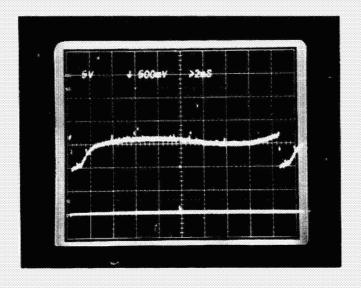


Average inhibited signal

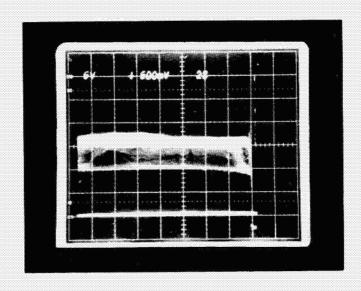
Average response (-13 Output level



Device Number JPL 9 Device Type $400 \times 400 \text{ buried channel}$ Light source 2854 $^{\text{O}}\text{K}$ Spectral filter 0.90 microns Average well population 50 % Temperature -39.5 $^{\text{O}}\text{C}$ Data rate 0.010 MHz Frame time $16 \times 10^3 \text{ms}$ Exposure time 250 ms

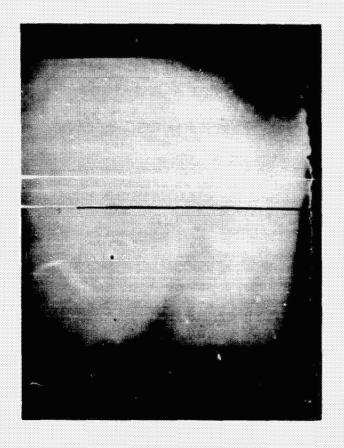


Oscilloscope presentation Video line number 200



Oscilloscope presentation Complete video frame

Device Number JPL 9 Device Type 400 X 400 buried channel



Light source 2854 $^{\circ}$ K

Spectral filter 0.466 microns

Average well population 50 %

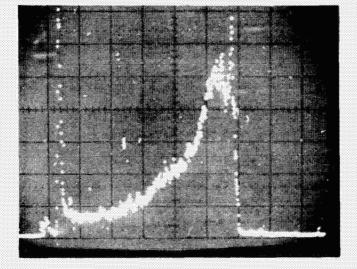
Temperature -39.5 $^{\circ}$ C

Data rate 0.010 MHz

Frame time 16×10^3 ms

Exposure time 250 ms

VIDEO MONITOR DISPLAY

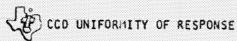


MULTICHANNEL ANALYZER DISPLAY

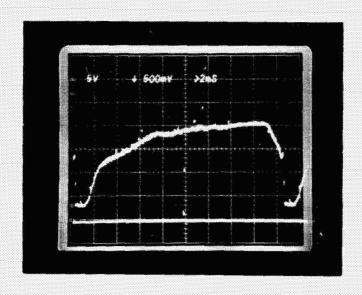
Average inhibited signal

Number of pixels

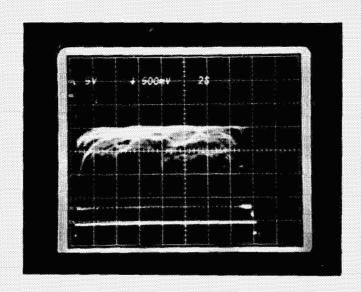
Avorage response C-15 Output level



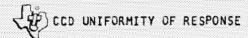
Device Number JPL 9 Device Type 400×400 buried channel Light source 2854 $^{\circ}$ K Spectral filter 0.466 microns Average well population 50 % Temperature -39.5 $^{\circ}$ C Data rate 0.010 MHz Frame time 16×10^3 ms



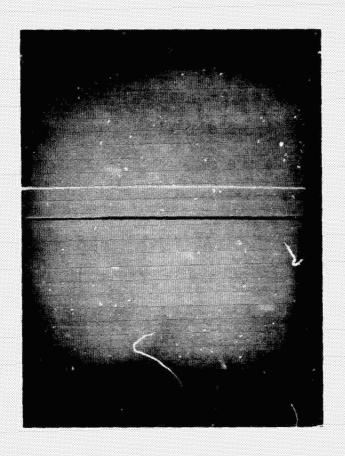
Oscilloscope presentation Video line number 200



Oscilloscope presentation Complete video frame



Device Number JPL 9 Device Type 400 X 400 buried channel



Light source 2854 $^{\circ}$ K

Spectral filter
None microns

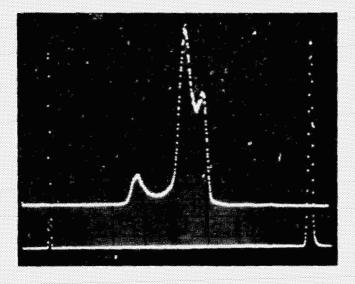
Average well population 30 %Temperature -39.5 $^{\circ}$ C

Data rate 0.010 MHz

Frame time 16×10^3 ms

Exposure time 250 ms

VIDEO MONITOR DISPLAY

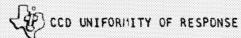


MULTICHANNEL ANALYZER DISPLAY

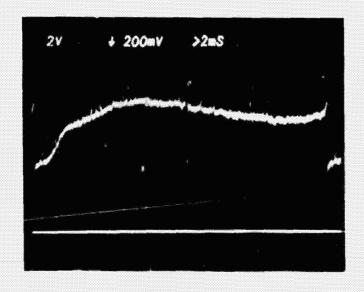
Average inhibited signal

Number of pixels

Average response C-17 Output level



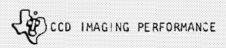
Device Number JPL 9 Device Type 400×400 buried channel Light source 2854 $^{\circ}$ K Spectral filter None microns Average well population 50 % Temperature -39.5 $^{\circ}$ C Data rate 0.010 MHz Frame time 16×10^3 ms



Oscilloscope presentation Video line number <u>200</u>



Oscilloscope presentation Complete video frame



Device Number		Device Type 400 X 400 buri	AND THE PROPERTY OF THE PROPER
Light Source	2854	K Spectral filter None	_ microns
Temperature			_ MHz
Frame time	16 X 10 ³	ms Exposure time 250	ms





CENTRAL RESEARCH LABORATORIES CCD Optical and Electrical Characterization Test Report

for

Customer JET PROPULSION LAB

Contract No. 953788

Device No. JPL 11 (136-5-4)

Device Type 400 X 400 buried channel

CCD OPTICAL AND ELECTRICAL CHARACTERIZATION TEST REPORT

۱.	CCD DEVICE NUMBER JPL 11 Pate 12-1-75
2.	DEVICE TYPE 400 X 400 buried channel
	Header type 40 pin DIP
	Active area 0.835 cm ² , pixel dimensions 0.9 mils X 0.9 mils
3.	OPERATING LEVELS in volts
	SUBS (substrate) -1 V Vref (precharge reference) 19 V S CLK (parallel clocks) 11 V Vref (drain voltage) 26 V S CLK (serial clocks) 11 V Vref (drain voltage) 26 V SID (serial input diode) 25 V SOG (serial output gate) 25 V Vref (drain voltage) 99 Close 90 Close
4.	AMPILIFIER CONFIGURATION used for the tests in this report Precharge Surface channel source follower
5.	SPECTRAL RESPONSE
Э.	SPECTRAL RESPONSE
	Quantum efficiency is $\frac{1.5\%}{50}$ at $\frac{0.4}{0.75}$ microns $\frac{0.75}{22}$ at $\frac{0.75}{1.0}$ microns.
	Frame readout mode, non shuttered, data rate 1 MHz, frame time 170 ms, temperature 25 °C, average well population 120 %.
	Note that quantum efficiencies are uncorrected for reflection.
6.	WIDEBAND RESPONSE
	a) Responsivity is 61 nanoamps/(microwatt) $$ b) $$ is 1.0 from saturation down to saturation divided by 100 . c) Sensitivity is 2×10^4 electrons/pixel at an exposure of $\mu \text{ J/m}^2$.
	d) Numerical integration of spectral response data at 90 % well population yields a sensitivity of 60 nanoamps/microwatt compared to the directly measured sensitivity of 61 nanoamps/microwatt at the same well population.
	Frame readout mode, non shuttered, data rate 1.0 MHz, frame time 163 ms, temperature 25 °C, 2854 °K source.
7.	SATURATION EXPOSURE
	a) Saturation exposure is $\frac{799}{\text{L}} \text{J/m}^2$, for $\frac{2854}{\text{C}} \text{ Source}$. b) A full well contains $\frac{1.6 \times 10^5}{\text{DOWN}}$ electrons.
	Saturation exposure measured as illumination level at which maximum

direction of blooming.

amplitude difference is achieved between light and dark bars of Nyquist frequency bar chart. Bars oriented perpendicular to the preferential

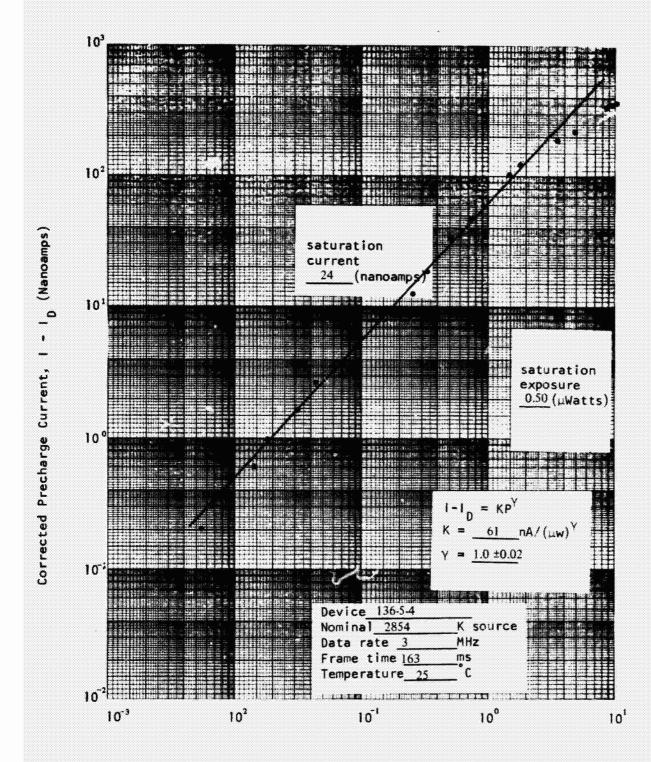
	C	C	C	•		T	I	*	S	T		F	l	F	•	0	1	R	*	ľ												
																							P									

7.	(continued)
	Frame readout mode, non shuttered, data rate 1.0 MHz, frame time 163 ms, temperature 25 °C.
8.	NOISE
	a) Number of RMS noise electrons is 300 . b) Noise equivalent exposure is 1.59 $\mu J/m^2$ for a 2854 °K source.
	Frame readout mode, data rate $\underline{1}$ MHz, frame time $\underline{163}$ ms, temperature $\underline{25}$ °C, off-chip amplifier bandwidth $\underline{2}$ MHz
9.	DYNAMIC RANGE
	Dynamic range is $\underline{510}$, defined as saturation exposure divided by noise equivalent exposure.
١٥.	DARK CURRENT
	Dark current measured by integration technique is 3×10^4 electrons/pixel/sec (0.92 nanoamps/m ²) at T = 24 °C, compared to 0.72 nano-amps/cm ² using precharge current measurements.
	Dark current measured by integration technique is $\frac{28}{100}$ electrons/pixel/sec $(0.71 \times 10^{-3} \text{ nanoamps/cm}^2)$ at T = $\frac{-40}{100}$ °C.
	Frame readout mode, data rate 1 MHz at T = 25 °C, 1 MHz at T = -40 °C. Frame time variable for integration technique, 163 ms for precharge measurement.
11.	DARK OUTPUT NONUNIFORMITY
	Dark output nonuniformity (standard deviation divided by the mean) is 0.35 at T = 25 °C.
	Frame readout mode, data rate 1.0 MHz, frame time 6257 ms
12.	RESPONSE NONUNIFORMITY
	Wideband response nonuniformity (standard deviation divided by the mean) is 0.22 for a 2854 K source.
	Spectral response nonuniformity is 0.17 for a 0.90 micron source, and 0.44 for a 0.466 micron source.
	Frame readout mode, shuttered, data rate 1.0 MHz, exposure time 163 sec, temperature 25 °C.
13.	BLEMISH COUNT
	Number of illuminated blemishes (pixels with a response less than $\frac{25}{\%}$ or more than $\frac{75}{\%}$ of full well with an average illumination level of 50% full well) is $\frac{749}{\%}$.

CCD T	EST	REPORT		
DEVIC	E NU	IMBER _	JPL	11

13.	(continued)
	Number of dark blemishes (pixels with an unilluminated output of more than 4 % of full well) is 7606 .
×	Frame readout mode, shuttered, data rate 0.01 MHz, exposure time 0.25 sec, source 2854 °K, temperature40 °C
14.	RESOLUTION
	Uncorrected square wave amplitude response at the Nyquist frequency
	a) for bars perpendicular to the serial register
	47 % at line 50 , bit 50 42 % at line , bit
	b) for bars parallel to the serial register
	47 % at line 50 , bit 50 46 % at line , bit 41 % at line 350 , bit 350.
	Frame readout mode, non shuttered, data rate 1.0 MHz, frame time 163 ms, temperature 25 °C, Strobe °K scurce, lens Wollensak aperture $F/8$, highlight illumination level 50 % full well.
15.	CHARGE TRANSFER EFFICIENCY
	Serial register charge transfer efficiency is 0.9999 for $50~\%$ signal pulse, $0~\%$ fat zero, data rate $1~$ MHz, temperature $25~$ °C.
16.	RESIDUAL IMAGE
	Residual image is less than $\underline{}$ 1 $\underline{}$ %.
	Exposure every other frame, highlight exposure greater than 75% full well, data rate $\frac{1}{\text{C.}}$ MHz, frame time $\frac{163}{\text{ms}}$ ms, temperature $\frac{25}{\text{C.}}$
17.	MEMBRANE FLATNESS over the active area is
	± <u>30 μm</u> microns measured at <u>25</u> °C.

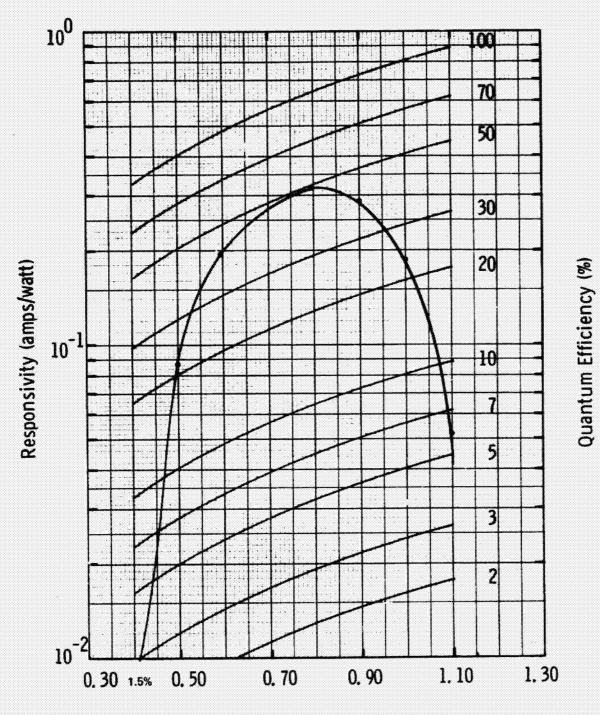
CCD SIGNAL TRANSFER



incident Power, P (μ Watts)

CCD SPECTRAL RESPONSIVITY

Device 136-5-4 (JPL 11)

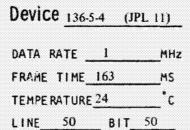


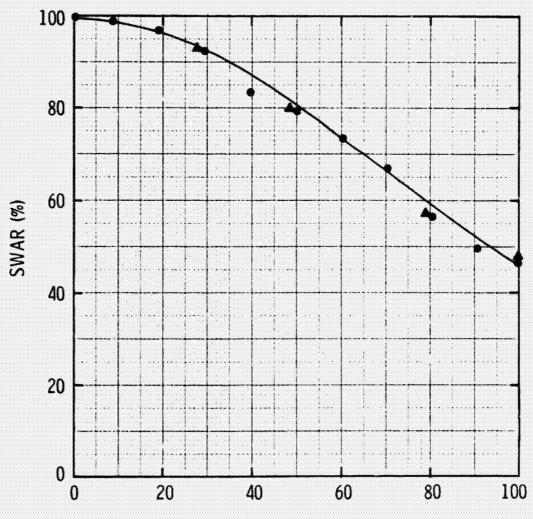
Incident Wavelength (µm)

DATA RATE 1.0 MHz
FRAME TIME 163 MS
TEMPERATURE 25 °C
D-6



CCD SQUARE WAVE AMPLITUDE RESPONSE





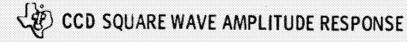
Spatial Frequency (% of Nyquist)

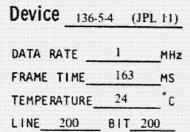
- BARS PARALLEL TO SERIAL REGISTER
- ▲ BARS PERPENDICULAR TO SERIAL REGISTER

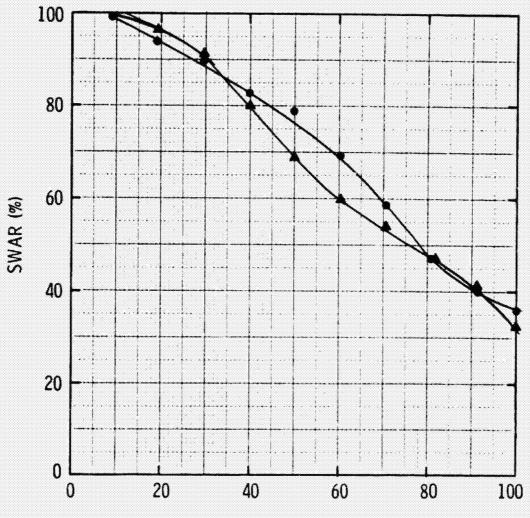
Strobed *K SOURCE - MICRON FILTER

LENS_ Wollensak

APERTURE







Spatial Frequency (% of Nyquist)

- BARS PARALLEL TO SERIAL REGISTER
- A BARS PERPENDICULAR TO SERIAL REGISTER

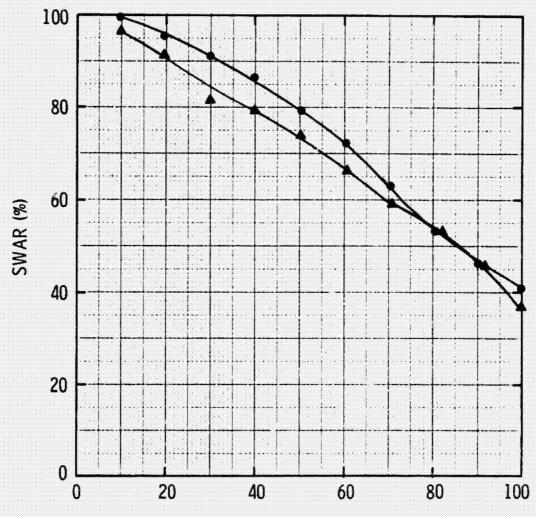
Strobed K SOURCE MICRON FILTER
LENS Wollensak

APERTURE 1/8



CCD SQUARE WAVE AMPLITUDE RESPONSE

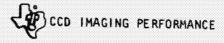
Device 136-5-4 (JPL 11) DATA RATE ____I MHz FRAME TIME 163 MS TEMPERATURE 24 LINE 350 BIT 350



Spatial Frequency (% of Nyquist)

- BARS PARALLEL TO SERIAL REGISTER
- BARS PERPENDICULAR TO SERIAL REGISTER

Strobed K SOURCE	MICONN CILTED
THE STATE OF THE S	MICRON FILTER
LENS Wollensak	
~ L ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' '	
APERTURE f/8	

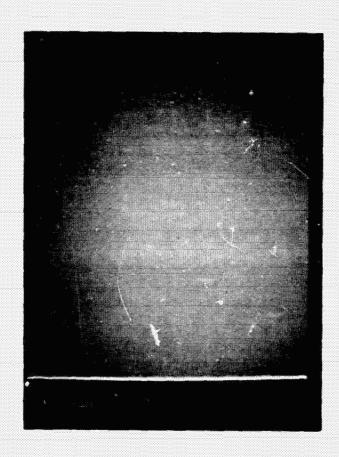


Device Number _1	136-5-4 (JPL	<u>11</u>) D	evice Type <u>400</u> 2	X 400
	2854		Spectral filter	- microns
Temperature	-40	°c	Data rate 0.01	MHz
Frame time	16,250	ms		

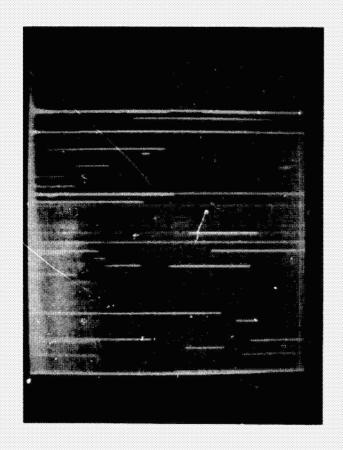


CCD IMAGING PERFORMANCE DARK BLEMISH ISOLATION

Device Number	JPL 11	Device T	ype <u>400 X 4</u>	00 Buried	Channel
Light Source	None	°K Spectr	al filter	None	microns
Temperature	40		ate <u>1.0</u>		MHz
Frame time	652	ms	30.00		

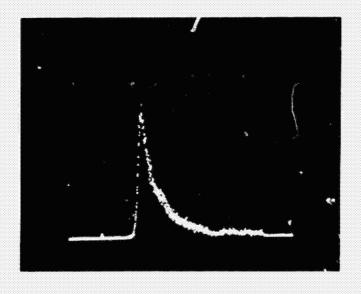


Device Number JPL 11 Device Type 400 X 400



Temperature 25 Oc Data rate 1 MHz Frame time 6257 ms

VIDEO MONITOR DISPLAY



MULTICHANNEL ANALYZER DISPLAY

Average inhibited signal

Number of pixels

Average dark signal D-12

Output level

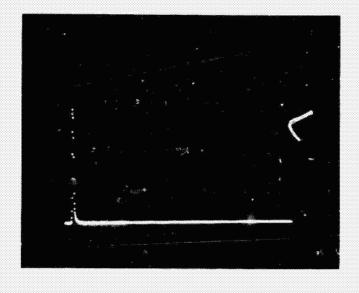
15 POOR

Device Number JPL 11 Device Type 400 X 400



Temperature __40 °C Data rate 0.01 MHz Frame time 16.25 seconds

VIDEO MONITOR DISPLAY

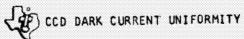


MULTICHANNEL ANALYZER DISPLAY

Average inhibited signal

Number of pixels

Average dark signal D-13

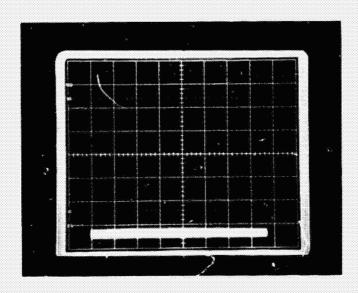


Device Number JPL 11 Device Type 400 X 400 Temperature -40 C Data rate 0.01 MHz	
Device Number JPL 11 Device Type 400 X 400	
Device Number JPL 11 Device Type 400 X 400	
Device Number JPL 11 Device Type 400 X 400	
Device Number JPL 11 Device Type 400 X 400	
Device Number JPL II Device Type 400 X 400	
Device Number JPL II Device Type 400 X 400	
Device Number JPL II Device Type 400 X 100	
Device Number JPL II Device 1/PC 133 II	
Device Adminer St. 11 Device 1/P	
DEVICE RUMBET	
DEVICE	
0	
Δ	

Frame time 16 sec



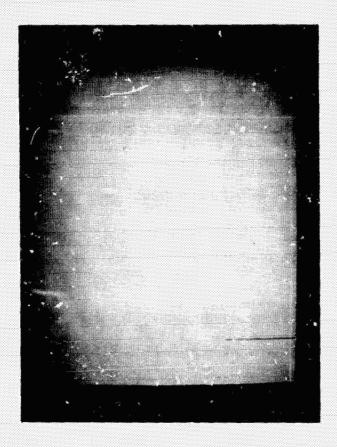
Oscilloscope presentation Video line number $\underline{200}$



Oscilloscope presentation
Complete video frame
[)-14



Device Number JPL 11 Device Type 400 X 400



Light source 2854 $^{\rm O}{\rm K}$ Spectral filter microns

Average well population 50 %Temperature -40 $^{\rm O}{\rm C}$ Data rate 0.01 MHz

Frame time 16.250 ms

VIDEO MONITOR DISPLAY



MULTICHANNEL MALYZER DISPLAY

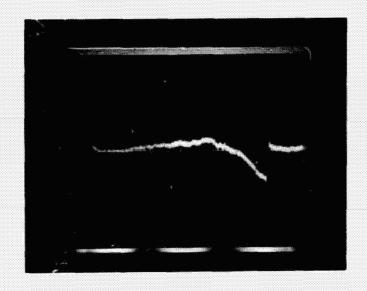
Average inhibited signal

Number of pixels

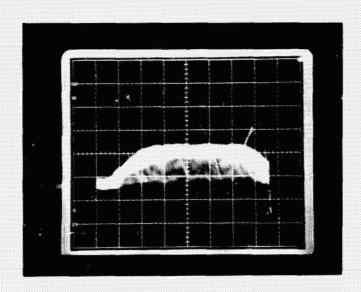
Average response

CCD UNIFORMITY OF RESPONSE

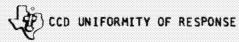
Device Num	nber <u>JPL II</u>	Device	Type	400 X	400	
Light sour	ce <u>2854</u>	K Spect	ral f	ilter _	eres.	microns
Average we	ell population	50	4	Tempera	ture	40°c
	0.01 MHz					



Oscilloscope presentation Video line number $\underline{200}$



Oscilloscope r esentation Comple wide: frame



Device Number JPL 11 Device Type 400 X 400



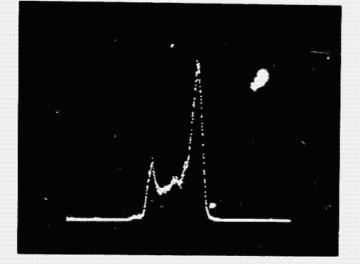
Light source 2854 Ox Spectral filter 0.9 microns

Average well population 50 %

Temperature -40 OC Data rate 0.01 MHz

Frame time 16,250 ms

VIDEO MONITOR DISPLAY



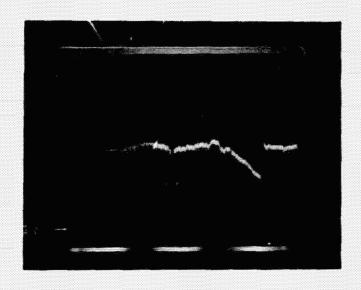
MULTICHANNEL ANALYZER DISPLAY

Number of pixels

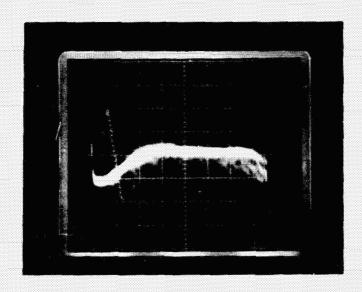
Average inhibited signal Average response D-17



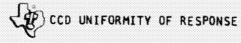
Device Number	- <u>JPL 11</u> (Device Type	400 X 400	
Light source	2854 ^O K	Spectral	Filter <u>0.90</u>	microns
Average well	population _	50 %	Temperature	_40 °C
			16 sec	



Oscilloscope presentation Video line number 200



Oscilloscope presentation Complete video frame



Device Number JPL II Device Type 400 x 400



Light source 2854 OK

Spectral filter
__466 microns

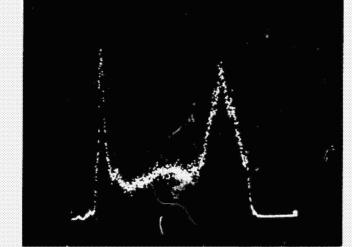
Average well population
__50 %

Temperature __40 OC

Data rate __01 MHz

Frame time 16250 ms

VIDEO MONITOR DISPLAY

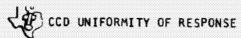


MULTICHANNEL ANALYZER DISPLAY

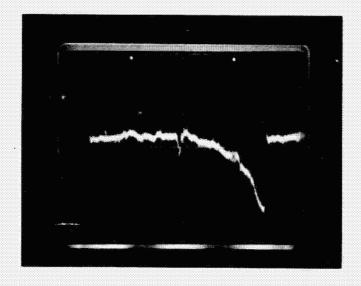
Average inhibited signal

Number of pixels

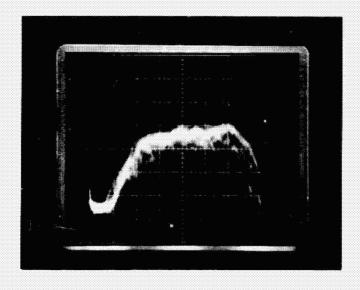
Average response D-19



Device Number JPL 11 Device Type 400×400 Light source 2854 K Spectral filter 0.466 microns Average well population % Temperature -40 C Data rate 0.01 MHz Frame time 16 sec



Oscilloscope presentation Video line number 200



Oscilloscope presentation Complete video frame



CENTRAL RESEARCH LABORATORIES CCD Optical and Electrical Characterization Test Report

for

Customer JET PROPULSION LAB

Contract No. 953788

Device No. JPL 12 (1-18-8)

Device Type 400 X 400 buried channel

CCD OPTICAL AND ELECTRICAL CHARACTERIZATION TEST REPORT

1.	CCD DEVICE NUMBER JPL 12	Date <u>12-1-75</u>
2.	DEVICE TYPE 400 X 400 buried channel	
	Header type 40 pin DIP	
	Active area 0.836 cm ² , pixel dimensions 0	<u>.9</u> mils X <u>0,9</u> mils
3.	OPERATING LEVELS in volts	
	SUBS (substrate) P CLK (parallel clocks S CLK (serial clocks) SID (serial input diode) SOG (serial output gate) V (precharge pulse amplitude) SUBS (substrate) V ref (drain value) V gg V gg V gg	charge reference) 17 V n voltage) 26.5 bias)
4.	AMPLIFIER CONFIGURATION used for the tests in this Buried channel source follower	report Precharge
5.	SPECTRAL RESPONSE	
	Quantum efficiency is $\frac{6.2\%}{58\%}$ at $\frac{0.4}{0.75}$ microns $\frac{22.3\%}{0.75}$ at $\frac{10}{0.75}$ microns.	
	Frame readout mode, non shuttered, data rate frame time 170 ms, temperature 25 °C, a population 80 %.	
	Note that quantum efficiencies are uncorrected for	reflection.
6.	WIDEBAND RESPONSE	
	 a) Responsivity is 68 nanoamps/(microwatt)^γ b) γ is 1.0 from saturation down to saturat c) Sensitivity is 1 × 10⁴ electrons/pixel at an end 100 μJ/m². d) Numerical integration of spectral response data population yields a sensitivity of 68 nanopared to the directly measured sensitivity of microwatt at the same well population. 	xposure of at <u>80 %</u> well amps/microwatt com-
	Frame readout mode, non shuttered, data rat frame time170_ ms, temperature25_	e 1.0 MHz, °C, 2854 °K source.
7.	SATURATION EXPOSURE	
	a) Saturation exposure is $915 \mu J/m^2$, for b) A full well contains 2.5×10^5 electrons. c) Blooming first occurs DOWN the channels.	2854 ^O K source.
	Saturation exposure measured as illumination level amplitude difference is achieved between light and frequency bar chart. Bars oriented perpendicular t direction of blooming.	dark bars of Nyquist

E-2

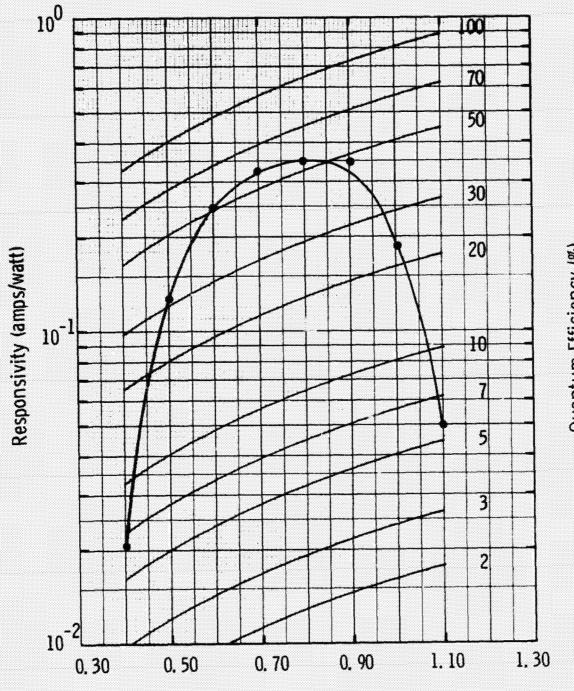
CCD TE	ST R	EPOR	T
DEVICE	NUM	BER	JPL 12

	DEVICE NUMBER
7.	(continued)
	Frame readout mode, non shuttered, data rate 1.0 MHz, frame time 170 ms, temperature 25 °C.
8.	NOISE
	a) Number of RMS noise electrons is 340 . b) Noise equivalent exposure is 1.5 $\mu J/m^2$ for a 2854 $^{\circ}$ K source.
	Frame readout mode, data rate 1 MHz, frame time 163 ms, temperature 25 °C, off-chip amplifier bandwidth 2 MHz
9.	DYNAMIC RANGE
	Dynamic range is $\underline{590}$, defined as saturation exposure divided by noise equivalent exposure.
10.	DARK CURRENT
	Dark current measured by integration technique is 1.2×10^{5} electrons/pixel/sec (3.07 nanoamps/cm ²) at T = 24.4 °C, compared to 2.6 nanoamps/cm ² using precharge current measurements.
	Dark current measured by integration technique is $\frac{74}{100}$ electrons/pixel/sec $(2.3 \times 10^{-3} \text{ nanoamps/cm}^2)$ at T = $\frac{-40}{100}$ °C.
	Frame readout mode, data rate 1.0 MHz at T = 24.4 °C, 1.0 MHz at T = -40 °C. Frame time variable for integration technique, 163 ms for precharge measurement.
11.	DARK OUTPUT NONUNIFORMITY
	Dark output nonuniformity (standard deviation divided by the mean) is 0.65 at T = 25 °C.
	Frame readout mode, data rate 1.0 MHz, Frame time 1820 ms
12.	RESPONSE NONUNIFORMITY
	Wideband response nonuniformity (standard deviation divided by the mean) is 20.7% for a 2854°K source.
	Spectral response nonuniformity is 0.49 for a 0.466 micron source, and 0.2° for a 0.90 micron source.
	Frame readout mode, shuttered, data rate 0.01 MHz, exposure time 0.25 sec, temperature -40 °C.
13.	BLEMISH COUNT
	Number of illuminated blemishes (pixels with a response less than $\frac{25}{\%}$ or more than $\frac{75}{\%}$ of full well with an average illumination level of 50% full well) is $\frac{15,800}{}$.

13.	(continued)
	Number of dark blemishes (pixels with an unilluminated output of more than 4% of full well) is 9.2×10^3 .
	Frame readout mode, shuttered, data rate MHz, exposure time 0.25 sec, source 2854 $^{\circ}$ K, temperature -40 $^{\circ}$ C.
14.	RESOLUTION
	Uncorrected square wave amplitude response at the Nyquist frequency
	a) for bars perpendicular to the serial register
	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$
	b) for bars parallel to the serial register
	$\frac{41}{\%}$ at line $\frac{40}{200}$, bit $\frac{40}{200}$ $\frac{46}{\%}$ at line $\frac{350}{350}$, bit $\frac{350}{350}$.
	Frame readout mode, non shuttered, data rate 1 MHz, frame time 163 ms, temperature 25 °C, Strobed °K source, lens Wollensak aperture $1/8$, highlight illumination level $1/8$ % full well.
15.	CHARGE TRANSFER EFFICIENCY
	Serial register charge transfer efficiency is $\frac{0.9999}{1.0}$ for $\frac{50}{\%}$ signal pulse, $\frac{0}{25}$ fat zero, data rate $\frac{1.0}{1.0}$ MHz, temperature $\frac{25}{1.0}$ C.
16.	RESIDUAL IMAGE
	Residual image is less than $1 $ %.
	Exposure every other frame, highlight exposure greater than 75% full well, data rate 1.0 MHz, frame time 163 ms, temperature 25 °C.
17.	MEMBRANE FLATNESS over the active area is
	± 32 microns measured at 25 °C.

CCD SPECTRAL RESPONSIVITY

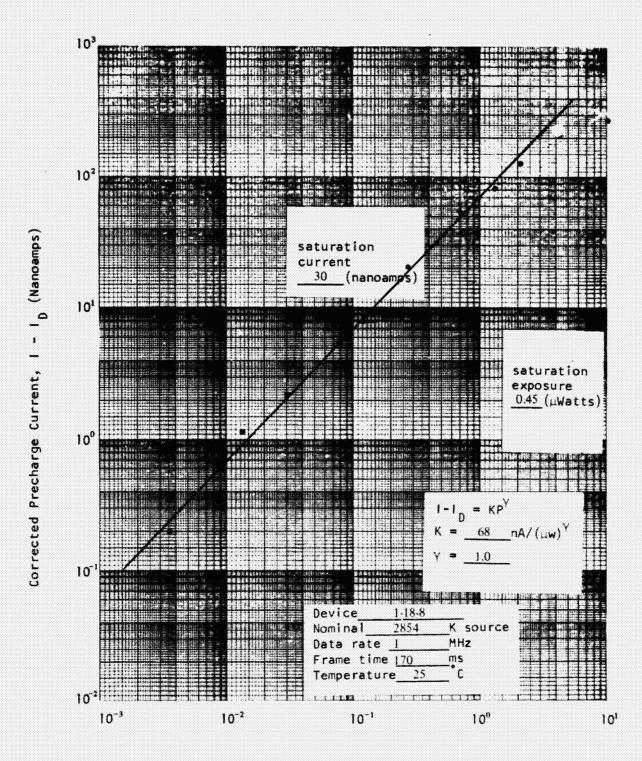
Device 1-18-8



Incident Wavelength (µm)

DATA RATE 1 MHz
FRAME TIME 170 MS
TEMPERATURE 25 °C
1:-5

CCD SIGNAL TRANSFER

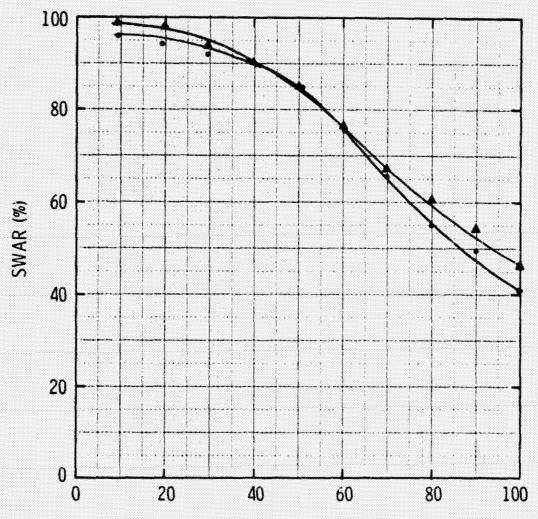


Incident Power, P (µ Watts)



CCD SQUARE WAVE AMPLITUDE RESPONSE

Device 1-18-8 DATA RATE ____1 __MHz FRAME TIME 163 TEMPERATURE 24 LINE_40____BIT_40_



Spatial Frequency (% of Nyquist)

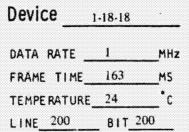
- BARS PARALLEL TO SERIAL REGISTER
- A BARS PERPENDICULAR TO SERIAL REGISTER

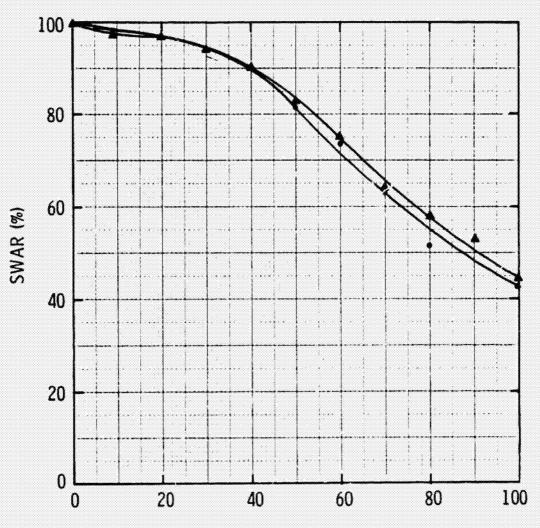
Strobe *K SOURCE MICRON FILTER

LENS____Wollensak

APERTURE 1/8





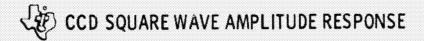


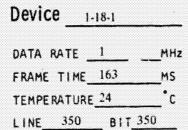
Spatial Frequency (% of Nyquist)

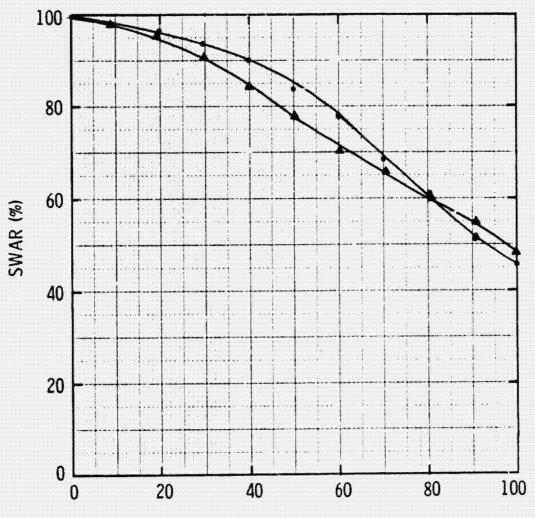
- BARS PARALLEL TO SERIAL REGISTER
- ▲ BARS PERPENDICULAR TO SERIAL REGISTER

Strobe K SOURCE MICRON FILTER
LENS Wollensak

APERTURE 1/8







Spatial Frequency (% of Nyquist)

- BARS PARALLEL TO SERIAL REGISTER
- ▲ BARS PERPENDICULAR TO SERIAL REG: TER

Strobe K SOURCE ____MICRON FILTER

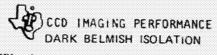
LENS Wollensak

APERTURE 1/8

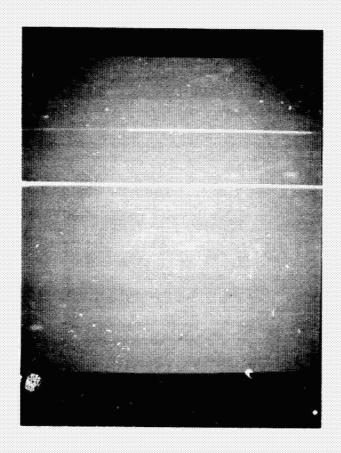


Device Number	JPL 12	Device Type _	400 X 400	
Light Source	2854	*K Spectral fi	lter	microns
Temperature	40	*C Data rate _	0.01	MHz
Frame time	16,250	ms Single Frame E	XDOSHIP	··········





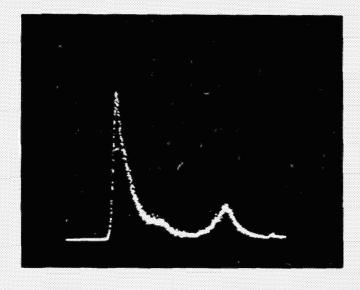
Device Number	JPL 12	Device Type	400 X 400	
Light Source		°K Spectral filt	er	microns
Temperature	-40	°C Data rate	1	MHz
Frame time	652	ms		



Temperature $\frac{25}{}$ OC Data rate $\frac{1}{}$ MHz Frame time $\frac{1825}{}$ ms

NOT TAKEN PRIOR TO DEVICE DELIVERY

VIDEO MONITOR DISPLAY



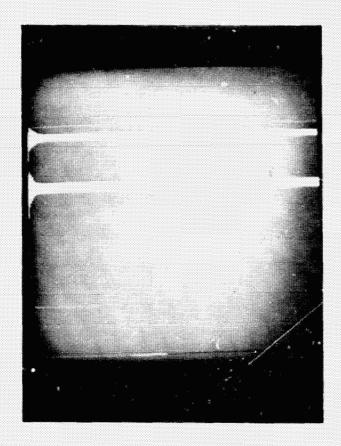
MULTICHANNEL ANALYZER
DISPLAY

Average inhibited signal

Number of pixels

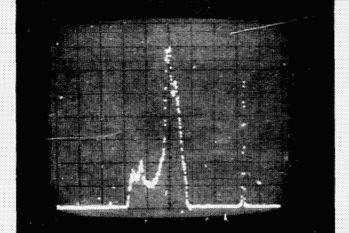
Average dark signal 1-12

Device Number JPL 12 Device Type 400 X 400



Light source 2854 CK Spectral filter ___ microns Average well population Temperature <u>-40</u> Data rate 0.01 MHz Frame time 16,250 ms

VIDEO MONITOR DISPLAY



MULTICHANNEL ANALYZER DISPLAY

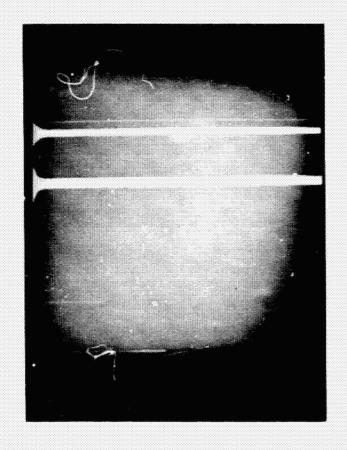
Average inhibited signal

Number of pixels

Average response 1-15



Device Number JPL 12 Device Type 400 X 400



Light source 2854 $^{\rm O}$ K

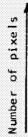
Spectral filter 0.9 microns

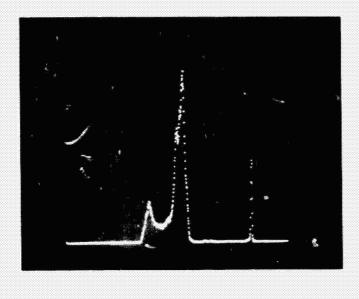
Average well population 50 %Temperature -40 $^{\rm O}$ C

Data rate 0.01 MHz

Frame time 16,250 ms

VIDEO MONITOR DISPLAY



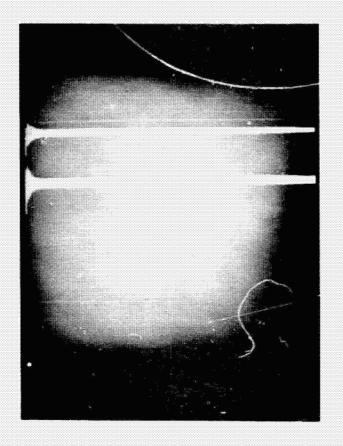


MULTICHANNEL ANALYZER DISPLAY

Average inhibited signal

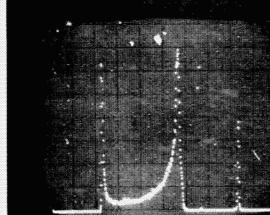
Average response

Device Number <u>IPL 12</u> Device Type <u>400 X 400</u>



Light source 2854 $^{\rm O}{\rm K}$ Spectral filter 0.466 πi πi

VIDEO MONITOR DISPLAY



MULTICHANNEL ANALYZER DISPLAY

Average inhibited signal

Number of pixels

Average response

DEVELOPMENT OF A 400 x 400 ELEMENT, BACKSIDE ILLUMINATED CCD IMAGER

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Texas Instruments Indorporated - Dallas, Texas 75222

ABSTRACT. Thinned, backside illuminated CCD imagers with 400×400 resolution elements have been fabricated using a double level anodized aluminum electrode system. These imagers have been developed for application to deep space photography where array read out rates of about 10 kHz and operating temperature near -40°C are envisioned. The performance of the 400×400 will be discussed and comparisons made to the operating parameters of a smaller 160×100 array fabricated with the same technology.

INTRODUCTION

heveral CCD technologies have been successfully applied to fabricate large area imaging arrays. 1-3 Illumination may be incident on the front, or electrode side of the array, but interference and absorption in either polysilicon or metal oxide electrodes can limit performance. Backside illumination, where radiation is focused on the planar back surface remote from the CCD electrodes, gives uniform and high spectral responsivity. Backside illumination 1-7 requires however that the CCD be thinned to about 10 µm to provide high resolution.

Large area CCD arrays are being considered for application in deep space photography where the requirements are such that the imager should operate at low data rates (~ 10 kHz) which requires device cooling (~ -40°C) to reduce thermally generated dark current during the long read out sequence. In this application the self-canned CCD may replace the conventional electron beam scanned vidicon. However, the processing complexity of the CCD as compared to the vidicon presents formidable problems in obtaining high quality, defect free devices which are greater in area than present commercial MOS integrated circuits.

This paper describes the development at Texas Instruments of a three phase 400 x 400 thinned, backside illuminated CCD array. Double level anodized aluminum technology

is utilized. The performance of a 160 x 100 array was discussed recently, ⁶ and in this paper we extend this discussion to the 400 x 400 imager. Both arrays have essentially the same serial-parallel-serial organization. Some of the processing details of particular concern with large arrays will be discussed.

DESIGN AND FABRICATION

The 400 x 400 is an n-channel, threephase (3¢) CCD, typically fabricated on 10-15 ohm-cm p-silicon. The resolution element size is 0.9 x 0.9 mil² which requires that each parallel and serial electrode be 0.3 mil in width. The channel width in the parallel section is 0.7 mil with 0.2 mil channel stop regions for an active area of 360 x 360 mil 2 on a 496 x 496 mil 2 chip of silicon. First and second level aluminum electrodes are isolated by about 2500 Å of Al₂O₃ formed by first level anodization. The structure is shown schematically in Figure 1 where it is apparent that a given phase occurs alternatively on first and second level electrodes. A photomicrograph of the corner of the array showing the output amplifier is shown in Figura 2. Since in the 30 design, each level is formed at an independent step in the CCD process, integration under a single parallel phase could possibly introduce line to line variation in the video output. Oscilloscope photographs showing several video lines are shown in Figure 3. Figure 3a indicates

video resulting from integration under ϕ_1 only and Figure 3b shows video after integration under both ϕ_2 and ϕ_3 . The line pairing, which is a feature of the 3 φ design is completely eliminated by using two electrodes. Square wave amplitude response (SWAR) data, giving resolution performance of the imager, is more reproducible using the two electrode scheme.

The second level electrodes overlap those on the first level by 0.05 mils to give a completely sealed electrode system. This allows buried channel array operation with high charge transfer efficiency (CTE). This design leaves 0.2 mil separation between electrodes which is the minimum that can reliably be opened by conventional wet etching technique. To maintain the design overlap of 0.05 mil in both parallel and serial sections presents formidable difficulties in both optical photomask generation and slice processing. CCD processing requires nine photomask levels which must be registered with each other, although of course, some are more critical than others. Random variations inherent in the generation of the master masks, which are due to mechanical limitations, can amount to ±0.015 mil and this can significantly affect a design overlap of 0.05 mil. The design overlap must also be maintained over many repeated arrays on the working photomasks used in processing. For processing on two inch diameter silicon slices, six to seven bars can be used while for three inch processing, 21 bars can be used.

A second factor which impacts device yield is the occurence of random defects in the photomasks such as accidental bridging between two channel stops (nonfatal) or between two metal electrodes (fatal). Individual treatment to eliminate these defects is often necessar, on the master reticle, These defects can be due to imperfections in the SiaNa used for the working masks or to dust particles in related processing and individual treatment is again used in most cases to remove most of these defects. In spite of these problems, however, it has been found that the design tolerances can be maintained over sufficiently wide fields so that processing can be performed on three inch silicon slices. At the present time device performance in so far as it is effected by photolithography, does not appear to be significantly affected by location on a processed slice. Extension to larger arrays, for which

the tolerance must be maintained over larger areas will be a progressively more difficult problem.

The 400 x 400 is designed to operate in the full frame imaging mode. An upper and lower output serial register is provided to allow forward or reverse array operation which increases device yield in the event of a maifunction of one of the on-chip output ampliflers. The array is divided electrically into four independent 100 x 400 sections so that a fatal processing defect in one section does not preclude operation of a partial array. This design feature allows an increased amount of performance data from a processed 'ot to be obtained for evaluation purposes. All electrical inputs necessary for array operation can be brought to bond pads along two edges of the CCD chip. Thus each 400 x 400 chip can be cut with a few mils of the two remaining array edges to allow a 800 x 800 mosaic to be made with the loss of only 5-10% of the active area.

The output from the CCD is by a simple precharge amplifier with reset switch (buried channel) and source follower (generally surface channel). For generation at 10 kHz follower load, resistors of up to 50 K are possible to reduce on chip power dissipation and membrane heating while maintaining low MOSFET noise.

Bond pads are extended some 50 mils from the active array so that the edges of the thinned silicon can extend outside this area but still leave a thicker 25 mil rim for membrane support. Thinning is performed by chemical etching techniques in which either a selected chip or complete slice can be thinned. The resulting membrane surface is highly reflective and can readily be coated with an antireflection (AR)/passivating layer of SiO. Although the membrane is generally somewhat nonplanar due to process-induced stress, device performance does not appear to be affected, even by repeated temperature cycling between 24°C and -40°C. A photograph of a CCD mounted in a 40 pin dual in line header is shown in Figure 4.

Burled channel operation of the array is necessary to achieve high performance at all points in the array. A 0.5 to 1.0 µm deep channel is formed by implanting phosphorus and a CTE > 0.9999 is measured in the serial register with 8-10 V clocks and no electrically introduced fat zero. Equally good CTE

In the parallel section is inferred from the square wave amplitude response (SWAR) data and is also measured by electrically injecting a pulse into the upper serial register and transferring through the parallel section to the power output amplifier.

CCD device processing generally makes use of conventional MOS techniques. p* channel stops and n+ diodes are formed by boron and phosphorus diffusion, respectively. Typical gate oxide thickness for the CCD's is 1350 - 500 Å. The buried channel is then formed by the phosphorus implant and subsequent drive in diffusion. This process is critical to obtain low dark current imagers. After first level metal patterning, the metal is protected by a layer of photoresist (vias) in certain areas which must connect to subsequent second level metal electrodes. Vias eliminate the need for less reliable n⁺ diffused tunnels as a means of interconnection for the electrode structure and allows all electrodes to be brought out on the same side of the array (Figure 2). The exposed metal is anodized and interconnects which had been required for electrical continuity during anodization are removed. Second level metal is then patterned to give a completely sealed electrode system. Detailed inspection of the first level pattern after etching generally revealed undesirable accidental bridges between adjacent metal electrodes due to either resist contamination during processing or to photomask defects. These would result in intralevel shorts if not removed prior to anodization. Pinholes in the anodic oxide which isolates first and second level electrodes will result in interlevel shorts. Anodization is a self-healing process and the quality of the interlevel isolation is very high. Nevertheless, metal defects are the dominant failure mode for our CCD's. Pinholes in the gate insulator are also fatal defects and considerable effort has been mode to grow high quality SiO, layers. Dry oxidation between 1000°C and 1100°C, with and without HCl impurity doping and steam oxidation at 950° have been investigated as well as the influence of chemical and vapor cleaning techniques on the pinhole density in the gate oxide layer. At present, the CCD gate is grown by steam oxidation and pinhole densities well below 1/cm2 have been achieved. The formation of pinholes appears to result from nonrandom defects or particles at the silicon surface prior to oxidation. Over the range 1000 Å to 1500 Å, the pinhole density does not

appear to depend strongly on oxide thickness.

The thermally generated array dark current in the buried channel arrays can be very low (I nA/cm), provided bulk gettering processes are applied in processing. At these levels the dominant dark current contribution is generated at the surface rather than in the bulk silicon as evidenced by a weak dependence of array dark current on clock voltage. Storage times to reach full well of 15 sec at 24°C and about three hours at -40°C have been achieved with the smaller 160 x 100 array. The incidence of localized dark current spikes in these deices is essentially zero. Since the generation rate for these spikes does not decrease with temperature as does the bulk silicon contribution. long storage times (or low dark currents) at reduced temperature require low defect density devices.

IMAGER PERFORMANCE

The successful use of large area CCD imagers in any application requires that an array meet many performance criteria simultaneously. In particular, low dark current with high uniformity must be combined with high uniform spectral responsivity to optical radiation. This latter parameter is of particular concern because large pixel to pixel nonuniformity in response may require excessive data reduction programs to allow maximum information to be obtained from the array. High CTE will result in maximum SWAR across the array while the backside illuminated geometry will provide the highest responsivity and quantum efficiency. Other parameters, such as their membrane planarity, will impact the final design of the optics which focus the image onto the CCD surface.

Operation of a 400 x 400 array at 10 kHz requires a read out time of 16 sec versus 1.6 sec for the 160 x 100. The read out sequence must be performed in the dark to avoid image streaking. Low data rates also streak out any individual blemished pixels so that defects which appear strongly localized at 3 MHz are not as well defined at 10 kHz. While this will improve uniformity of response, it limits the dynamic range of the imager. Imagery taken with the 400 x 400 at -40°C with a 0.25 sec integration time and a 10 kHz read out is shown in Figure 4.

Performance parameters for two representative 160 x 100 buried channel arrays

have been presented elsewhere. In Table I,

TABLE I

Characteristics of Typical (Best in Brackets) 160 x 100 Arrays and Initial 400 x 400 Arrays

<u>CTE</u>	160 x 100: 0.9999 (8V Clocks)	400 x 400: 0.9999 (8V Clocks)
Dark Current 24°C -40°C	6.5 (1.8) nA/cm ² 0.008 (0.0011) nA/cm ²	7.4 nA/cm ² 0.19 nA/cm ²
Responsivity	90 mA/watt (No AR)	72 mA/watt (No AR)
SWAR at the Nyquist Frequency Parallel to Serial Perpendicular to Serial	49% (Array center) 50% (Array center)	39% (Center) 36% (Center)
Uniformity of Response (-40°C)	0.12 (0.08)	0.16
Dark Uniformity (-40°C)	0.50 (0.14)	0.43

representative average and best parameter values are given for 160 x 100 devices based on experience gained during a twelve-month period. Also shown are values for initial buried channel, 400 x 400 arrays. Excellent charge transfer characteristics are evidenced by high CTE and SWAR. For the larger array, there is only a few percent decrease in SWAR going from a pixel near the output to one far from the output.

The 160 x 100 array design has on chip preamplifiers with MOSFET loads which result in heating of the membrane and this can limit device storage time. The storage times quoted above were determined by disabling the amplifiers during a variable integration period and reading out the serial register rapidly at I MHz. Membrane heating from the source follower on the 400 x 400 can also be observed at long integration times where typical on chip power dissipation is 20-40 milliwatts for a 5 KO off chip load. This lead to increased dark current nonuniformity. These effects can be minimized however by positioning the amplifier on the thick silicon rim or by using a higher load resistor (say, 50 KQ) which is certainly permissable for 10 kHz data rates. As indicated in Table I, initial 400 x 400's, which were processed on three-inch silicon, typically showed a higher density of localized dark current blemishes than expected from recent 160×100 's. The contribution of these blemished pixels to array dark current does not decrease like $T^{3/2} \exp(-Eg/2kT)$ as predicted and higher than expected dark current is measured at -40°C. These localized spikes

may be due to defects in the silicon substrate, residual impurities in the silicon, or implant damage which is not completely annealed. Subsequent processing improvements are expected to significantly reduce these localized dark current sites to the low levels seen in the smaller arrays.

The backside illuminated CCD should be characterized by highly uniform responsivity since optical radiation is focused on an etched silicon surface. However, membrane thickness non uniformities often result in bands of higher (or lower) sensitivity. Uniformity of response, as measured by sampling each pixel with a multichannel analyzer and defined as the standard deviation divided by the mean, has been limited to about 8%. Variations in the backside accumulation process used at the membrane surface also lead to non uniformities in response, particularly at shorter wavelengths. Devices with 70% quantum efficiency at 4000 A have been fabricated but at present an average value is in the range 10 - 20%. High QE devices often show some variation in responsivity as the temperature is decreased from 24°C to -40°C which is generally not observed in the lower QE devices. Surface passivation with AR coatings of SiO have been applied to the membrane surface and appear to stabilize device response against long term variations. It is expected that improved etching techniques together with passivation will eventually result in response uniformity of 5%

CONCLUSIONS

High performance, backside illuminated CCD arrays have been demonstrated in a configuration sufficiently large to have application in a spacecraft environment. Operation at low data rate and -40°C appear to be compatible with the thinned CCD technology. Further improvement in array performance is predicted and improved packaging techniques, particularly aimed at increasing stability of the thin membrane, will be implemented to allow eventual application in the spacecraft camera system.

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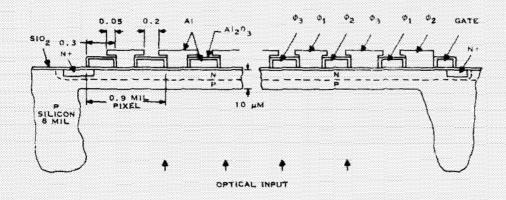


Fig. 1. Schematic of backside illuminated, double level metal CCD.

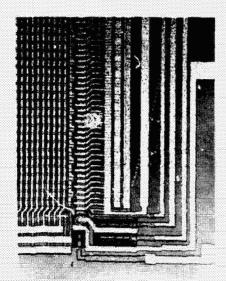
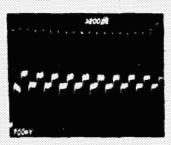


Fig. 2. Photomicrograph of one corner of the 400 x 400 array showing both serial and parallel busing from one side. The output amplifier is a reset switch and source follower.



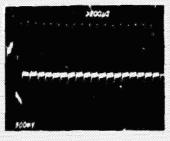


Fig. 3. Line video output from CCD using ϕ_1 parallel for integration (a) and ϕ_2 + ϕ_3 for integration (b).



Fig. 4. Imagery of the IEEE Standard taken with a 400 x 400 at $24\,^{\circ}\text{C}$ and 1 MHz data rate corresponding to a frame time of 163 msec.

LARGE-AREA CCD IMAGERS FOR SPACECRAFT APPLICATIONS*

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Backside illuminated CCD imagers with 100 X 160 resolution elements have been fabricated using double-level metal technology. Detailed study of the optical performance of such arrays has been performed between 24°C and -40°C using data rates from 10 kHz to 1 MHz. A 400 × 400 array is presently being fabricated.

I. INTRODUCTION

Large-area charge-coupled device (CCD) imagers can be fabricated with any of several existing technologies (Refs. 1, 2, 3). Since a completely sealed electrode structure is very desirable to optimize device electrical performance, many arrays use polysilicon electrodes which are sufficiently transparent to allow optical radiation to enter the active region of the CCD. Electrode absorption and interference effects related to the device structure itself can result in a degradation of the optical performance, particularly at short wavelengths. Illumination of the CCD from the backside (Ref. 4) eliminates this problem but requires that the silicon chip be thinned to about 10 µm for optimum performance. This paper will discuss the characteristics of backside illuminated, three-phase (3 \$\phi\$) (Ref. 5), buried-channel imagers fabricated using the double-level anodized aluminum technique (Ref. 6). A completely sealed structure with high charge transfer efficiency (CTE) and optimum optical responsivity is obtained. The electrical and optical performance of arrays with 160 \$\times\$ 100 resolution elements will be presented to confirm that this technology can be successfully

^{*}This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration, under Contract No. NAS 7-100.

applied to fabricate high-performance CCD imagers. The unique aspects of the double-level, backside illuminated structure will be discussed with emphasis on a 400×400 array presently being fabricated.

II. DESIGN AND FABRICATION

The 160 \times 100 imager is an n-channel device designed to have a resolution element size of 0.9 \times 0.9 mil². The organization is serial-parallel-serial, which allows the input of electrical signals to the parallel section. A double-level aluminum metallization separated by approximately 2500-Å Al_2O_3 forms the transfer electrode structure. Three-phase clocking is used so that in both the parallel and serial sections of the array a given phase occurs alternately on first-level and second-level metal electrode (Ref. 5). The signal charge packets are transferred to the (ϕ_3) output serial register electrodes through a composite gate region of width 0.3 mil. Overlap of first- and second-level electrodes is nominally 0.05 mil to achieve a 0.9 \times 0.9 pixel. This requirement places extremely tight tolerances on photomask perfection, particularly for 400 \times 400 size arrays.

An output amplifier is provided for both upper and lower seri- registers to allow forward or reverse operation of the imager. This can increase array yield in the event of a malfunction of one amplifier. A balanced sample-andhold design takes the precharge output from a source follower through a sampling MOSFET and to a second source follower, giving an amplifier bandwidth greater than 10 MHz. On-chip load MOSFETs are used in this design. A correlated clamping circuit is provided at the upper serial output to investigate on-chip low-noise video processing. This amplifier has a bandwidth of about 1 MHz. A micrograph of the 325 x 325 mil² chip is shown in Figure 1. Bond pads are extended some 50 mils from the active area so they remain over the thick silicon after a region slightly bigger than the array itself (90 × 144 mil²) has been thinned. Thinning was performed by chemical etching either after the individual chips had been mounted on ceramic 40-pin headers or by etching a whole slice using an etch mask around each individual array. In this latter case, the slice was then scribed into individual chips and each subsequently mounted on headers. Either technique can provide uniformly thin membranes of thickness 10-12 um. The surface of the membrane is highly reflective, although a light surface haze is sometimes found after removal from the etch. Membrane

stability is such that repeated temperature cycles from 24°C to -40°C do not fracture the CCD. Distortion of the membrane is observed in some cases at -40° but can be minimized by avoiding temperature gradients.

The imagers were operated in the full frame mode, and the readout sequence occurred while light was incident on the device. To reduce streaking in the displayed image, the ratio of integration time to readout time should be \$3:1, and a 5-second exposure at an output rate of 10 kHz (1.6-second readout) was used at -40°. A shuttered mode of operation is simulated by illuminating with a short light pulse during the integrate period only, and the imagery of a 160 × 100 operating in this mode at 24° C is shown in Figure 2.

High charge transfer efficiency is achieved by using a phosphorus implantation to achieve a 0.5-1.0 μ m deep buried channel in nominally 10 Ω -cm p-type silicon. Typical buried-channel arrays operate at 6-8 volt clocks with a CTE of ≥ 0.9999 (measured in the serial register) with no electrically introduced fat zero. Equally good CTE in the parallel section is inferred from the squarewave amplitude response (SWAR) data discussed below. It does not appear that the transfer gate region to the output serial register is affecting array performance.

III. IMAGER CHARACTERISTICS

The successful incorporation of the CCD imager into a spacecraft system will require that a given array meet many performance specifications. High CTE and spectral responsivity must be combined with a low blemish count and dark current. Uniformity of both responsivity and dark current are very desirable. The arrays discussed in this paper are intended for operation at long exposure times and a 10-kHz data rate at -40°C. Array dark current is expected to decrease with the temperature T at $T^{3/2}$ exp $(-E_g/2kT)$ or a factor of 895 between 24°C and -40°C. Storage times of ≈ 200 seconds should therefore be possible at -40°C without appreciable filling of the potential wells.

Performance parameters of two buried-channel 160 X 100 arrays are indicated in Table 1. The consistent achievement of high CTE requires tight control over substrate resistivity and implant dose to achieve the desired buried channel. Any metallization defects, particularly in the serial output registers, will also degrade CTE from the optimum for the buried channel. Using a voltage contrast mode with a scanning electron microscope allows correlation of

such defects with array CTE and allows processing optimization. There does not appear to be any significant effect of temperature (25°C to -40°C) or frequency (10 kHz to 1 MHz) on the measured transfer efficiency.

The dark current I_D of the buried-channel arrays is in the range 10-20 nA/cm² at room temperature as measured by a picoammeter in the precharge line of the output amplifier. While this method of measurement is generally reliable at 25°C, it fails completely at lower temperatures, where I_D becomes lower than the CCD leakage currents. Our measurements (Table 1) at -40°C are taken using an integration technique that allows the dark current to build up over a long period (~200 seconds at -40°C) to give a significant well population which results in an easily measured video voltage output. The CCD/amplifier is calibrated using a (large) current injected at the input diode in a separate measurement. This technique gives a decrease of 1000× between 24°C and -40°C in satisfactory agreement with that predicted above. In contrast, the precharge technique gives a decrease of 80-100, which merely reflects the degree of spurious dc leakage current from the CCD and ceramic package.

One advantage of the backside illuminated mode is high responsivity and smooth spectral responsivity (Figure 3). The log-log plot of signal current versus incident power has a slope (γ) of 1 ±0.1 under all operating conditions. The wideband responsivity to 2854-K radiation with no AR coating is 90 mA/watt with a 70% quantum efficiency at 4000 Å. Decreasing temperature to -40° appears to decrease the responsivity at all wavelengths below about 6000 Å by about 30% as measured on a device with peak QE of 40% at 8000 Å. This effect may be related to a change in surface recombination velocity and suggests that a passivation layer or antireflection coating be applied to the thin membrane surface. For a $100-\mu J/m^2$ exposure at the array during a 5-second exposure time, the ratio of signal to dark current (-40°C) implied by the data is 18.6 for 2854° radiation.

The squarewave amplitude response of the imager taken with a high-contrast bar chart is shown in Figure 4 out to the Nyquist frequency $f_{\hat{N}} = 21.9$ line pairs/mm. The results in Figure 4 were taken at 1 MHz and -40°C, since detailed comparisons at 10 kHz (where data is less accurate) and 24° and -40° show no consistent change in the SWAR. This result would indicate that any distortion of the thin CCD membrane at -40°C is not sufficient to affect device resolution. High array CTE is reflected by measuring a constant SWAR across

the array (Figure 4), and only a very small SWAR loss can be attributed to CTE degradation. At f_N , the SWAR is 40% and 30% for bars parallel and perpendicular respectively to the serial register. The lower value for perpendicular bars is due to a bandwidth limitation in the external electronics in the 1-MHz data and is not a CCD effect. Without this limitation (device II), the SWAR for parallel bars is found to be 0.04 below the perpendicular value.

An estimate of the SWAR for device I can be made as follows: Using a substrate resistivity of 5 Ω -cm, and a buried-channel dose of 1.5 \times 10¹² cm⁻² and drive-in of $2\sqrt{D}t=0.6~\mu m$, where D = diffusion coefficient for implanted phosphorus and t = drive time, one can calculate the depletion layer width to be 3.2 μm from the SiO₂-Si interface for 8-volt clocks. If the substrate has been thinned to 10 μm , this results in a neutral bulk layer thickness of 6.8 μm . By first substituting these values into the Crowell-Labuda formula (Ref. 7) for diffusion MTF, which has been shown by Seib (Ref. 8) to be an adequate approximation to the CCD case in essentially all instances; next, multiplying by the pixel collection aperture MTF ($\sin \pi f d/\pi f d$, d = pixel pitch = 0.0229 mm) and the lens MTF; and finally, substituting this total MTF function, $R_0(f)$, into the formula for SWAR,

SWAR(f) =
$$\frac{4}{\pi} \sum_{m=0}^{\infty} \frac{(-1)^m}{2m+1} R_0[(2m+1)f]$$

one finds the SWAR at the Nyquist limit ($f_N = 21.9 \text{ lp/mm}$) to be 0.53 for illumination naving a 0.8- μ m wavelength, the wavelength of peak sensor response. This is somewhat above the experimental value of 0.40 but possibly results from the monochromatic assumption in the model.

Isolated light blemishes in the arrays have been reduced to a low level by bulk gettering and annealing processes (Figure 2). Bulk lifetimes after processing are ~50 µsec, and interface states at the Si-SiO₂ boundary are $<10^{10}/\text{cm}^2$ -eV. However, the uniformity of response to 2854-K illumination has been found to depend on the thinning process itself. Nonuniform thinning can result in bands of higher (or lower) sensitivity, which in some cases correlate with a light surface haze remaining after the chemical thinning. The uniformity of the imager response (and also of dark current) is determined by sampling each pixel video

with a multichannel analyzer, and is defined as the standard deviation divided by the mean. This parameter is equal to 0.19 at 5% of full well and 0.14 at 50% of full well for a 2854-K source measured at 10 kHz and -46°C. Uniformity of 0.08 both for 2854-K and 4000-Å radiation at 24°C have been measured in a device at the 20% saturation level (Table 1). Uniformity of dark current is 0.96 at -40°C and 10 kHz. Device II is more uniform at 24°C but degrades at low temperature. It should be noted however that the array dark uniformity is affected by an apparent heating effect in the membrane from the on-chip load MOSFETs.

Preliminary measurements of dynamic noise of isolated pixels using the balanced sample-and-hold amplifier indicated about 400 electrons of noise at 1 MHz and -40°C, which is considerably higher than expected from a buried-channel device. More recent results (Ref. 9) using improved measurement technique indicate a noise as low as 67 electrons at 24°C and 1 MHz. However, even with a noise level of 400 electrons, the dynamic range of the imager is 3500:1 (full well 1.6 x 10⁶ electrons with 7-volt clocks).

IV. DISCUSSION AND CONCLUSIONS

The performance of the 160 X 100 arrays appears sufficiently promising to allow fabrication of a larger $3 \, \phi$, double-level imager of similar basic design. Fabrication of this array is in progress, and several problems peculiar to this 0.5 × 0.5 chip have become apparent. Photomask perfection is extremely difficult to maintain over such large areas, and a single defect in a metal level mask can cause a fatal intralevel metal short in the array. This problem can be minimized in slice processing but at the expense of additional steps. The integrity of gate oxide is important, since a 400 × 400 will have 101,000 mil² of thin oxide. Defect (pinhole) levels of <0.5 cm² have been observed on test slices using dry-wet-dry or HC l doped oxides. The integrity of anodic A l_2 03 is well recognized, but pinholes do exist and will give rise to interlevel shorts. This effect is minimized by the 0.05-mil overlap, but care must be exercised to maintain some overlap in order to allow buried-channel operation. These yield loss mechanisms are all expected to be of prime importance for the 400 X 400. The performance of such an array is expected to be comparable to that of the 160 × 100. Uniformity of thinning and membrane planarity for areas near 1 cm² may require further development, and some form of support for the membrane may be necessary to maintain planarity. The uniformity of response and of dark

current may also depend on silicon slice perfection and the effectiveness of bulk gettering over extended areas.

In conclusion, the results presented have shown that the double-level anodized aluminum technique can be used to fabricate high-performance 3 ¢CCD imagers which operate at reduced temperatures and 10-kHz data rates.

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Table 1. Performance parameters of two buried-channel 160 × 100's

	I	п
CTE	0.9999 (7-V clocks)	>0. 9999
Saturation level	1.6 × 106 electrons at 7 V	2 × 10 ⁶ electrons
Dark current	0.0078 rA/cm ² (-40°C)	_
	7.8 nA/cm ² (+24°C)	6.5 nA/cm ²
Responsivity (2854 K)	90 mA/watt (24° C)No AR coating	99 mA/watt
Quantum efficiency (4000 Å)	70% (24°C)	10% (24°C)
SWAR		
Parallel to serial	40%	37%
Perpendicular to serial	29%*	41%
Signal to dark current ratio (100-µJ/m² exposure for 5 sec at -40°C)	18.6	_
Response uniformity	0.14 (-40°C)	0.08 (24°C)
	50% full well	20% full well
Dark uniformity	0.96 (-40°C)	0.24 (24° C)

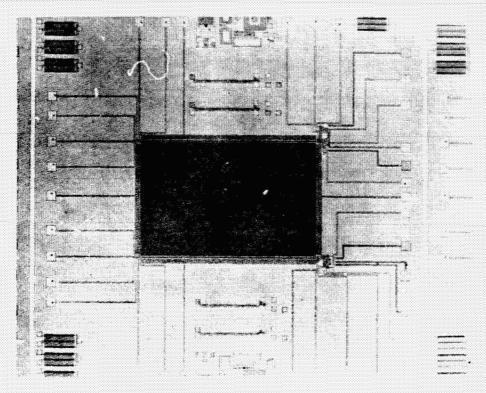


Figure 1. Photomicrograph of 160 \times 100 CCD imager (Active area is 144 \times 90 $\rm mil^2$ and total chip is 322 \times 325 $\rm mil^2$.)

160 x 100 BURIED CHANNEL IMAGER

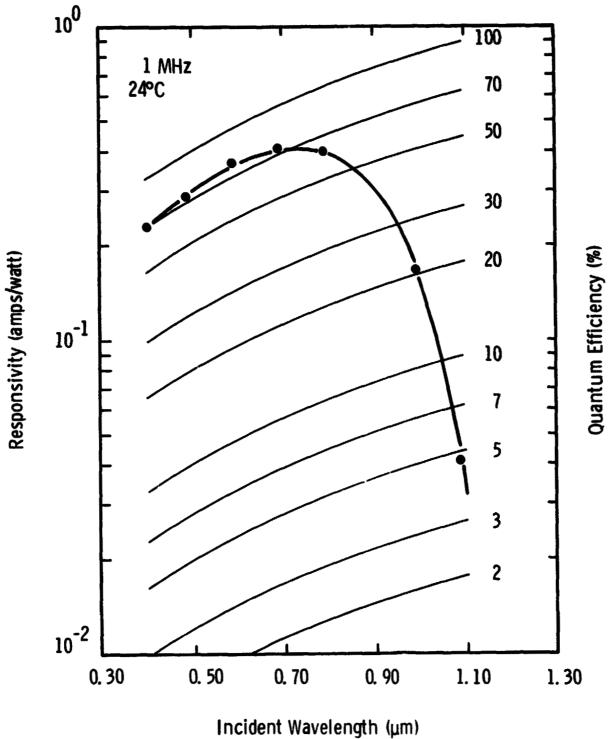


DATA RATE 1 MHz
TEMPERATURE 22°C
ILLUMINATION STROBED

Figure 2. Imagery at 24°C with buried-channel array using a strobed source to simulate shuttered operation

COMMATY OF THE

160 X 100 BURIED CHANNEL



Spectral responsivity of 160×100 array (At -40°, there is an apparent decrease in responsivity below about 6000 Å by about 30%.) Figure 3.

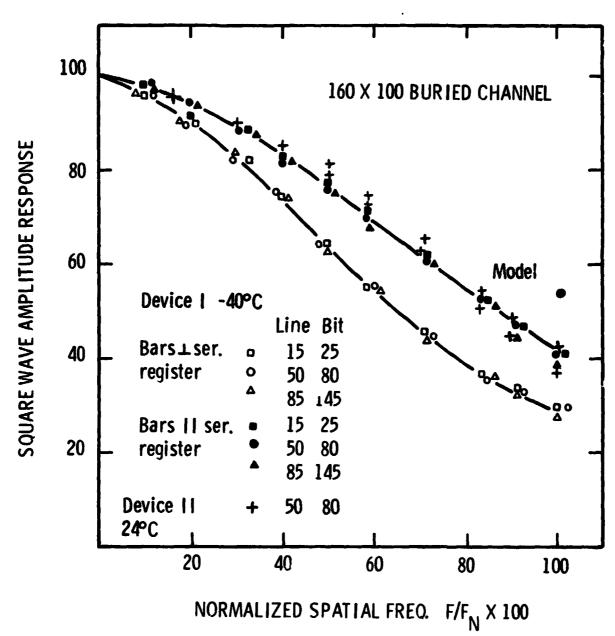


Figure 4. Squarewave amplitude response using a high-contrast bar chart (Essentially no change across the array is observed. The corrected value at the Nyquist frequency indicates the theoretical model for SWAR discussed in the text for device I.)

INTRODUCTION

A. LARGE CCD AREA IMAGERS

At the beginning of the JPL area imager program in 1974, several CCD device processing parameters were not we'll known - in particular, whether a pixel size as small as 0.9 x 0.9 mil was possible for the double level electrode metallization scheme. Experience with the smaller 160 x 100 imager indicated that the problems could be solved but extension to the larger 400 x 400 proved to place severe restrictions on photomask quality. Nevertheless, it has proved possible, with extreme care in photomask production, to fabricate excellent quality 400 x 400 CCDs. In view of this achievement, the question arises as to the next size increment for an area imager. Factors effecting this step and recommendations based on experience gained during the JPL program will be discussed in this report.

Several techniques are available to the large bar designer. For the 400 x 400, Texas Instruments presently makes use of optical generation of photomasks which are then used in contract printing on either two inch or three inch diameter silicon slices. One alternate system for mask generation makes use of electron beam generated masks which are then usually followed by projection printing on the silicon slice. E-beam generation has been reported to yield a 'perfect' mask more readily than optical generation but at present Texas Instruments does not have the capability for e-beam generation for arrays as large as required for CCD imagers. Use of projection, rather than contract printing, preserves the master mask from damage due to contact with the silicon slice. This damage can destroy a minute piece of geometry, and if the same mask is used again, may cause fatal defects in the CCD. Projection printing has not been used in the current JPL program because of the high cost and unavailability of such equipment for CCD fabrication. Projection printers are, however, in operation in other

processing areas at Texas Instruments. Their use for CCD processing should reduce the low defect density presently tolerated in the working copies of the master photomask.

Even if high quality photomasks for a larger device can be fabricated, the yield of defect free CCDs resulting from the MOS processing itself will be reduced from that for the 400 x 400. Fatal defects from processing (oxide pinholes and metal defects) have been controlled to such a degree that the present yield of 400 x 400's on three inch silicon slices is about the same as that encountered early in the JPL program with the much smaller 160×100 . Thus processing technology has improved significantly and the defect density for the 160×100 has been considerably reduced during this time. This impressive development provides a degree of confidence in going even further to an 800 x 800 although comparable improvements will be more difficult to achieve because the technology has already been optimized in several areas and little improvement is now expected without intensive effort. Alternate approaches to fabrication of a large monolithic imager are the two phase (20) CCD and electron beam processing. At the midpoint of the present program with JPL, a 30 imager was recommended for the 400 x 400 because experimental results at that time for 20 CCDs were not impressive - in particular, a high CTE, 20 phase device had not been demonstrated. The situation is now somewhat more favorabe for 20 as will be indicated below and such an array should be reconsidered since it offers an overall size advantage.

One of the major impact areas for large CCD imagers is in the field of solid state TV cameras. The resolution requirements for the commercial TV application requires an array about 512 x 360 and there is then no strong need to increase the array size except for the more limited high resolution applications. While development of an array about this size could benefit from paralled interest in entering the solid state TV camera market place and the resulting technical development which would occur, similar interest in larger Jevices, such as the 800 x 800

will be marginal and this could slow the general development of a monolithic device of this size.

Since a CCD is a parallel-serial device, the information stored in the location farthest from the output must transfer many more times than that near the output. Unless the paralled charge transfer efficiency (CTE) is very high, this can lead to degredation in the array modulation transfer function (MTF) across the device. For the three phase 400×400 array, a maximum of 2400 transfers are made which increases to 4800 for an 800×800 . Since the MTF falls approximately as $\exp(-N\varepsilon)$ where N is the number of transfers each of inefficiency ε , the array MTF uniformity required sets a limit on the array size. The parallel CTE for the buried channel 400×400 appears to be at least 0.9999 and may even be higher. Assuming 0.9999, the variation, corner to corner, across a 400×400 will be from unity to $\exp(-0.24) = 0.79$ or to $\exp(-0.48) = 0.62$ across an 800×800 . It is possible that a mosaic of $400 \times 400^{\circ}$ would give superior resolution uniformity.

PRESENT IMAGER DESIGN

The present CCD imager developed for JPL is a three phase 400×400 resolution element device with a resolution cell size of 0.9 x 0.9 mil. This implies an active area of 360×360 mil for the parallel section of the array. Output serial registers, including bus lines for interconnection take an area of 5×360 mil and parallel bus lines occupy 4×360 mil so that the relevant device area over which tight geometrical tolerances must be maintained in processing is 370×368 mil. Output amplifiers (reset switch and source follower) can be designed with somewhat relaxed tolerances but the output circuitry only occupies about $8 \times 8 \text{ mil}^2$ at two corners of the array.

In Figure 1, the electrode structure of the three phase, double level aluminum CCD is shown. The most important geometrical factors are (1) a design overlap of 0.05 mil for the second level over first level electrodes and (2) the 0.2 mil wide

separation between each second level electrode. It is mandatory that some electrode overlap is maintained over the whole array to achieve good buried channel operation and the design of 0.05 mil is the minimum which can be used if any overlap is to be expected after metal processing. The 0.05 dimension can be increased to relax processing and photomask tolerances but only at the expense of the separation of second level electrodes. Such a solution is not possible however because the 0.2 mil second electrode gap is the minimum which can be reliably opened using current aluminum wet etching techniques. Alternatively the overlap could be enlarged by increasing the pixel size which is also undesirable because it implies an increase in array area to maintain equivalent imager resolution.

PHOTOL I THOGRAPHY

The generation of photomasks for the 400 x 400 is performed by conventional optical techniques and has been found to require state-of-the-art fabrication by the Photomask Facility of Texas Instruments. The difficulties arise from 1) the extremely tight tolerances (0.05 mil overlap) which must be maintained over a large area (370 x 368mil), 2) the number of such bars which are stepped on the working photomasks and 3) the requirement for defect free mask geometry over large areas.

The generation of photomasks for a CCD imager (see Figure 2) is initiated by generating a computer tape containing all the design dimensions for each of the mask levels which will be eventually used in device processing. In the 400×400 design, ten levels are designed which must be registered with each other. At the present time the size limitation in this design phase is a bar of 999×999 mil. Design of geometry involving 0.01 mi; increments is possible. The computer tape, which has been iterated several times to correct design errors, is used in a D. W. Mann Pattern Generator to generate a master reticle containing

geometry of each required level, i.e., 10 reticles. Due to limitations in subsequent mask generation processes it is presently not possible to generate photomasks if a device is as large as the design limit of $999 \times 999 \, \text{mil.}$ The nature of the limitations will be outlined below.

The pattern generator can generate a reticle (geometry on a glass plate) as large as 4 x 4 inches. The reticle is then placed in a precision step and repeat camera with a reduction optical system of either 5x or 10x. The reduced image of the reticle (now the size of the final CCD) is imaged onto a glass plate which will be the master photomask and then this image is stepped and exposed again to generate an array of bars on the master. This master is then used in a contact printing to make working copies on glass plates which are used in device processing. At this step at the present time, there are two options available at Texas Instruments. The first is to generate a 4" x 4" reticle which is reduced by 10x to give a miximum working bar dimension of $400 \times 400 \text{ mil}^2$. At the present time a 5x reduction lens, which could be used with a 4" x 4" reticle to give a 800 x 800 bar is not available. Estimates of cost for such a lens (and camera) from Zeiss and Mann are well above \$100K. The second option is to use a $2\frac{1}{2} \times 2\frac{1}{2}$ " reticle and reduce by 5x to obtain a maximum bar size of 500×500 mil. This is the technique used for the 400 x 400, which is therefore at the limit of present system capability if a single reticle is to be used. As can be seen, the design of the bar must be limited to either 400 x 400 mil (Option 1) or 500 x 500 mil (Option 2) rather than the 999 x 999 mil design limit indicated earlier. A technique of generating more than one reticle for each level and then combining them in the step and repeat camera to compose a larger bar, termed Reticle Composition, is possible. This will be discussed separately since the process is not now routinely used at Texas Instruments and is also of questionable accuracy if two regions containing fine geometry (as in the parallel section of a CCD) are to be butted together.

The quality of the working photomasks strongly influences the quality of the processed CCD. Two quality factors have been found to be extremely difficult to control. The first is related to the dimensional accuracy of each individual bar and the distance between each bar on the master photomask. Since the CCD process requires registration of ten photomask levels to each other on the silicon slice being processed and this must maintain the design tolerances of 0.05 mil, such dimensional variation is very undesirable. Absolute bar dimensions depend critically on the focus of the optical system in the Step and Repeat Camera. It is difficult to maintain a given focus through 10 individual levels. Random mechanical errors in the step and repeat distance are specified as \pm 0.015 mil but a highly experienced operator can usually improve on this by scanning in a preferred sequence. These factors can result in loss of electrode overlap from one corner of a bar to the opposite corner and also to an unacceptable bar placement error, particularly at the edges of the bar array on the 4 inch square photomasks which are used for the 3 inch slice processing. At the edges of the array the limitations of the optical system become more apparent. The printing of working photomasks from the master mask can result in dimensional changes but this is generally not a severe problem. At the present time device yield does not appear to depend particularly on location, implying that acceptable masks, although requiring extreme care in fabrication, can be fabricated by the Texas Instruments facility.

The second factor which is important is the random defect level in the array geometry. An example of this, is that the metal level patterning masks must have no accidental bridging in the parallel section of the array because such bridging will give rise to a fatal defect in the CCD where two adjacent metal electrodes will be joined. One such defect can be fatal. A defect in the reticle is occasionally generated by the Pattern Generator but more usually particles in the photographic emulsions or chrome layers or Si_3N_4 defects

produce these effects. Hand crafting is used extensively for the 400 x 400 masks and even so, it is extremely difficult to obtain zero defects for all (21) of the bars used for 3" slice processing. These problems will increase as the area of the bar increases, but there will be a corresponding reduction in the total number of perfect bars which are required to fit on the silicon slice. However, the reduction in total bars processed for a given number of slices will of course, strongly impact the total device throughput.

ELECTRON BEAM GENERATED PHOTOMASKS

An electron beam can be focussed to a spot a few hundred angstrom units in diameter and then used to expose and define fine geometry in special e-beam resists. It is possible to generate excellent challty glass photomasks using the e-beam rather than using the more conventional optical techniques described above. For this particular CCD application, the array geometry would be about the same dimension but it appears that master masks of higher perfection can be generated using e-beam technique. These master masks are then used directly in a projection printing mode so no damaging contact with silicon slices occur in processing. At the present time Texas Instruments does not have the capability of generating masks of the size used for the 400 x 400 CCD imager. Smaller devices have successfully been made using e-beam masks and conventional MOS processing. It is expected that the capability for large bar generation will be developed. However, it is not clear what the size limitation will be, but it should be greater than 500 x 500 mil since the device pattern is written directly on the mask.

Due to the shorter wavelength of the electron relative to that of the UV optical radiation used in conventional optical photomask generation, much smaller geometry can be successfully defined by the e-beam. Features of 1 µm are easily achievable. Therefore, a CCD with much reduced pixel dimensions - perhaps

0.1 x 0.1 mil², can be designed. Such patterns may be directly written in special resist which is on the silicon slice itself although special processing is then mandatory to transfer the resist geometry to the silicon. Many of the techniques using the e-beam machine and subsequent device processing, are under development at Texas Instruments as well as in other laboratories. A review of Device Lithography, as well as several papers on the various approaches, has recently been published in the IEEE Transactions on Electron Devices, July 1975. For the above pixel dimensions a three phase 1000 x 1000 array would occupy 100 x 100 mil, but significant development will be required in processing for such a device.

RETICLE COMPOSITION

This is a process to overcome the 500 x 500 mil limitation on the size of the CCD bar (i.e., the present limitation to a $2\frac{1}{2}$ x $2\frac{1}{2}$ " reticle and a 5x lens). The process is not currently in use at Texas Instruments although Reticle Composition was used several years ago to fabricate successfully the photomasks for a linear 500 x 1, CCD shift register.

In the process, the computer tape from the design phase generates more than one reticle on more than one glass plate at the Pattern Generator. The final bar is composed from the reticles by appropriate placement at the Step and Repeat Camera. This would allow a significant increase in active array size, except for the difficulty of exactly joining the fine detail in the array on each reticle to maintain continuity of the mask geometry. Registration between levels would be even more difficult since the reticles of each level are composed separately. It is not thought possible to successfully use composition in the paralled section of a 0.9 x 0.9 pixel area imager. Such composition may be possible however, for CCDs which do not have such tight tolerances such as some single level designs. An alternative which is more realistic, involves firstly an array design which confines all fine geometry (containing all 0.05 mil tolerance)

to less than 500 x 500 mil so it can be put on a single reticle. This means approximately a 550 x 550 pixel array. Wide (≥ 1 mil) metal leads are extended away from the array about 2.5 mil to reach the 500 x 500 mil bar limit. Four more reticles, containing the continuation of these wide leads to band pads some 50 mils away are generated separately and the total bar composed in the Step and Repeat Camera. The composition errors are not as important now since the geometry to be butted is large (≥ 1 mil) and continuity of the bond lead should be maintained without much difficulty.

Since reticle composition is a non-standard process, fabrication of masks, although feasible with existing technology, will require longer and be somewhat more expensive than has been the case with the 400×400 .

PROCESSING LIMITATIONS FOR LARGE CCD IMAGERS

For the three phase, double level CCD imager there are two failure modes which significantly effect device yield ofter processing. These are pinholes in gate oxide and metal defects in the electrode structure. It has been determined from 400 x 400 and 160 x 100 data, that oxide pinholes are generally not random. That is, there is not a single area dependence of pinholes, as the size of the CCD array is increased. This means that the larger CCDs are not as difficult to make (only as regards pinholes) as would be expected on the basis of data on smaller area devices. Present results on the 400 x 400's suggest that it will be possible to fabricate a 550 x 550 with significant less yield loss than would be predicted from only the 2x gate oxide area difference between them. Extension to an 800 x 800 seems possible also from this viewpoint.

The second loss mechanism for the 30, double level metal CCD is metal defects, either interlevel or intralevel. The former results from pinholes in the interlevel isolation dielectric (Al_20_3) and the latter from random photoresist or photomask defects or etching non-uniformities during metal patterning. Both are fatal for the CCD and presently are the most significant loss mechanism in 400 x 400 processing.

It is not possible to isolate the two types of metal defect with dc probe data for the double level, $3\emptyset$ design. Experience with both the 160×100 and the 400×400 suggests that the loss due to these defects at the present level of technology is approximately proportional to the electrode area. At this time, the loss which we would predict for a 800×800 would prevent good bar fabrication. A 550×550 may be possible, but the yield would be reduced with current technology.

For the 400 x 400, about 20 bars are processed on a 3 inch diameter silicon slice and 6-7 on a 2 inch diameter slice. Present experience is that 3 inch processing is very desirable simply due to the larger number of bars which can be processed for a given number of slices. At present, twenty slices form a lot for processing on three inch material and ten slices for processing two inch. The number of bars are 400 versus 60. For a 550 x 550, we believe that three inch processing will be mandatory and then only about 10 bars per slice will be possible. For an 800 x 800, about 6 bars per slice seems achieveable. Even if the percentage device yield is not decreased (although in practice it will be however), this means that more than three times as many slices must be processed for a comparable number of 800 x 300's. A significant increase in the number of slices in processing would be mandatory for an 800 x 800 and even for a 550 x 550.

The pixel size of an imager can be reduced if two phase clocking is used to transfer charge rather than the present three phase method as in the 400×400 . Recent results at Texas instruments for a proprietary, 2 phase design. limear array indicate that buried channel operation with high CTE (> 0.9999) can be achieved. Early 20 CCDs had poor CTE which made them look unattractive for large area imagers. The pixel size for a 20 imager would have to be no larger than $0.6 \times 0.6 = 0.36 \text{ mil}^2$ in order to fabricate an 800×800 device within the present 500 mil bar limitation in the photomask shop. This could possibly be

achieved but certainly it will be at the expense of full well capacity. This latter is a feature of all 20 designs which must have a built in potential assymetry for directionality of charge transfer under one electrode. This reduces full well capacity under this electrode by 30-50%. High CTE, buried channel, 20 CCD registers, using pixel of 0.8 x 0.5 mil have been successfully operated at Texas Instruments. Present development is aimed at an operating register with a 0.6 x 0.3 mil pixel. Therefore, a large 800 x 800, 20 array with a pixel less than 0.36 mil² could readily be designed and would appear to have good probability for excellent performance. An additional advantage of the 20 design is that each phase is entirely on the same level of electrode metallization so that intralevel shorts are rot longer fatel defects. However, a successful, large area 20 array has not been built at this time. Nevertheless it seems to offer an excellent possibility of increasing the pixel density and providing a higher yield device.

ALTERNATIVE APPROACH TO LARGE ARRAYS-MOSAIC

An 800 x 800 CCD array can be achieved by placing four 400 x 400's in close proximity along two edges as indicated in Figure 3. In this arrangement there will be some loss in active area between each 400 x 400 which can be minimized by arranging the read out direction as shown. The 400 x 400 was designed so that the silicon chip can be operated using band pads on only two sides of the array so that the remaining two sides can be sawed to within several mils of the edge of the active area of the array. These sides may be then joined as shown. The total composite would be about 840 x 840 mils with an insensitive area of about 29,000 mil² compared to an active area of 518,000 mil², i.e., a loss of 6%. Each array would probably require a thick silicon rim only about 5 mil in width along the two sides which were sawed and the thinning window itself would require very shamply defined edges to maintain response uniformity to the last active line (or column) of the imaging section. Both these conditions appear at present to

be more readily achievable than the fabrication of a high performance monolithic 800×800 even though development will be required in mechanical sawing and etching control.

SUMMARY AND RECOMMENDATIONS

The extension of the present 400 x 400 CCD imager to a larger number of pixels will almost certainly result in some increase in device loss due to (a) photomask perfection and (b) processing induced fatal defects. As outlined in this report, these loss mechanisms are related to (a) the design tolerances and (b) general difficulty involved in processing very large MOS devices. Developments in array technology, possibly with the consideration of alternate CCD structures will be required to offset area increases and an increased number of silicon slices will need to be processed to achieve high performance in the final CCDs.

It does not appear that the present 400×400 can be increased in size to any significant degree using identical photomask technique to those being used to fabricate the present CCD imager.

The following discussion will give, in order of difficulty as seen at the present time, the preferred steps to increase the area of a monolithic CCD imager.

1. If a modest increase in size is required, for example to 550 x 550, reticle composition can be used with a high degree of certainty to compose the bar. Maintaining acceptable overlap tolerances over a larger *** will be however increasingly difficult. In the opinion of the Photomask Facility it should be possible, however the level of confidence is not 100%. The impact of processing induced defects will be important and will effect array performance in so far as less devices will be available from which to select arrays with optimum values of many parameters. Current array technology should however be adequate with some further development.

2. For an 800 x 800 imager, conventional photomask generation can be used only if a new optical lens system becomes available. If this occurs, the overlap tolerance required will be a severe problem which is difficult to discuss since extrapolations to this size are not expected to be reliable. Processing loss would be high and at the current level of our technology, the number of good devices processed is predicted to be insufficient to deliver high performance imagers. Significant increases in the number of slices processed would be mandatory since the bar would be about 820 x 820 mils. Use of projection printing to maintain the mask quality once masks were generated, would be very desirable.

Prior to the design of such a bar, consideration should be given to processing advantages of alternate electrode structures which eliminate intralevel metal shorts as fatal defects. It is also recommended that the reduced area of a 20 array design be considered since processing yield will certainly be enhanced by a smaller area device.

3. If the mosaic of four 400×400 's is acceptable, this solution to the problem of large number of pixels appears to be more readily achieved than a monolithic 800×800 . Predictions can be made with some degree of reliability from current experience with the 400×400 . The sawing of the CCD close to the active area does not appear to be inherantly difficult. The key problem in minimizing dead area between the 400×400 's is to obtain a sharp edge at the thinning window. Techniques to do this are presently under development.

B. SHORT WAVELENGTH RESPONSE OF BACKSIDE ILLUMINATED IMAGERS AND PREDICTED LOW LIGHT LEVEL PERFORMANCE.

One feature of the backside illuminated mode of CCD imaging is that optical radiation is incident on a uniform etched silicon surface. In some respects this provides superior performance to the front side illuminated CCD where interference effects in the electrode structure (which is partially transparent) and in the protective overcoat layer give non uniform spectral response. Electrode absorption can also limit responsivity. The recently developed transparent electrodes of Indium or Tin oxide may have less absorption but localized absorption bands could be present. The responsivity to broad band 2854°K radiation of Texas Instruments, backside illuminated imagers is routinely in the range 70-90 mA/watt, about a factor of two higher than frontside illumination with the more widely used polysilicon electrodes. Peak quantum efficiency is 65-70% at about 7000Å with no antireflection coating. Optimum backside accumualtion can result in 65% quantum efficiency at 4000Å for such imagers.

The performance of the backside illuminated device is particularly sensitive to (a) thickness uniformity of the thin (~10µm) membrane, (b) backside accumulation profile and (c) long term stability of the etched silicon backside surface. The short wavelength (4000Å) responsivity of the imagers has been found to depend strongly on these parameters and to show a fairly wide spread in absolute magnitude and uniformity. Figure 4 shows representative data for the best and average spectral response per 160 x 100 CCD's. Only a limited amount of data is presently available. The high quantum efficiency at 4000Å in the best devices suggests that useful response could be obtained at even shorter wavelengths than 4000Å.

However, extension of measurements below 4000A has not been made at the present time to determine how rapidly the QE decreases. At the present time experience with 160 x 100's indicates that the 65% blue response can not easily be achieved on a routine basis due to difficulty in controlling the (proprietary) Backside Accumulation Process. Experience indicates that a more representative number for the QE at 4000A, which can be achieved with a greater degree of certainty, is in the range 10-30%. Since 400 x 400 imagers are available in reduced numbers compared to the 160 x 100, due to processing induced defects, there are fewer of these large devices from which to select the arrays which come closest to the goals set out in the specifications. Therefore at the present time it seems reasonable that the 400 x 400's will have QE (4000A) between 10 and 30%. Further development is necessary to increase the control and reporducibility of the thinning/backside accumulation process. This is recognized as a key problem area for both EBS and direct view CCD imagers and is the focus of an internal program in the Central Research Laboratories. High GE at short wavelengths will be a (strong) function of the elched membrane surface potential as well as the accumulation profile and a surface passivation layer to fix the potential at the desired point will be highly desirable to maintain stability. A layer of silicon monoxide should be adequate and will also provide an AR coating to further improve response at the desired wavelength.

The longer term goal of extending CCD response to about 2500A would appear to be very difficult with present technology using a direct view sensor i.e. where the optical input occurs directly onto the silicon membrane surface. Further development may allow reproducible results

in this range but surface conditions will be critical since the absorpiton length at 2500A is $< 0.01\mu m$, and the response is predicted to be very small. As indicated above no experirental data is abailable for the CCD's, due partially to the unavailability at TI of light sources and calibrated detectors in this spectral region. A much more promising approach to achieving high performance in the near UV is to fabricate an EBS (electron beam scanned) imager, where the optical input is made to a photocathode which then generates electrons that are accelerated by at 10-15 kV potential to impact the CCD backside surface. Gains of 1000-2000 may be achieved in such an EBS mode. Recently a successful EBS tube has been demonstrated by NASA Goddard and by the Night Vision Laboratories using TI 160 x.100 CCD area imagers. Several photocathode/window combinations are available with response in the UV spectrum. The $Tri-alk/Si0_2$ has a QE of 20% from about 2500A to 5000A while a Bi-alk/MgF, has QE > 10% from about 1400A to 4000A (Figure 5). None of these have good response out to 9000A however.

An extensive study of the low light level (LLL) capabilities of both the direct view CCD and EBS CCD has been made by Texas Instruments for the Night Vision Laboratories (Contract DAAKO2-74-C-0359). The resulting comparisons are important since they indicate that at low light levels, (abou: 10⁻⁷ watts/meter²) the EBS sensor out performs the direct view sensor even when the latter is cooled to 210°K.

Since this discussion is concerned only with the ultimate results of this study, only a brief summary of these calculations is presented and then representative results are given - a detailed discussion is given in the above mentioned NVL Final Report. The LLL imager performance for a

CCD is based on a psychophysical model due to Rosell and Willson (Series of Reports from Westinghouse Defense and Electronic Systems to AFAL-TR-72-279, AFAL-TR-73-260 and AFAL-TR-74-104) for conventional imaging tubes. A disply signal to noise ratio $P_{\bar{D}}$ for imaging a black and white bar pattern is defined as

$$P_D = \frac{N_S}{N_D}$$

where N_S = number of signal photoelectrons = $N_{MAX} - N_{MIN}$

 N_{MAX} / N_{MIN} = equivalent number of photoelectrons generated within the image of a bright/dark bar during eye integration time $\tau_{\rm a}$.

 N_n = equivalent RMS number of noise electrons/bar image averaged over a bar pair and integrated over $\tau_{\rm p}$.

 $N_S = N_{MAX} - N_{MIN}$ can be expressed in terms of the modulation transfer function (MTF) or square wave—flux—response of the system at spatial frequency f and the average number of signal photoelectrons generated within the image of a bar during the integration period τ_e , averaged over a bar pair, N_{AV} .

 N_n can be written as $N_n = (N_{NP}^2 + N_{nS}^2)^{\frac{N_2}{N_P}}$ where N_{NP} is photoelectron noise due to optical input and N_{nS} is system noise. $N_{PP}^2 = N_{AV}$ and N_{nS} is the equivalent RMS noise electrons per bar added to the video so that $N_n = B(N_{AV} + N_{NS})^{\frac{N_2}{N_S}}$. The operator B takes into account changes in total noise produced by the system MTF's and is discussed in the NVL. Report. Rosell and Willson showed in a series of experiments that a bar pattern imaged on the sensor can just be resolved by an observer looking at a display when P_D for that pattern and sensor combination is about 2.5. The observer was allowed to adjust display contrast. In the CCD analysis

 P_{th} is conservatively taken as 3.0. The results presented below therefore show at what light level a displayed bar chart pattern of frequency f can be resolved by an observer i.e. at what light level a P_{D} of 3.0 is achieved for a particular f. f will not be given in line pairs/mm but rather in TV lines/picture height by multiplying by two times the CCD photosensitive height in mm. This was done to make the graphical data compatible with earlier work.

In order to express the total square wave flux response of the system at the bar chart frequency f, in terms of the total system MTF, expressions for the following components are obtained

- (1) Diffusion MTF
- (2) Secondary generation MTF (EBS only)
- (3) Pixel collection MTF
- (4) Transfer MTF
- (5) Lens MTF
- (6) Tube pretarget MTF (EBS only).

Diffusion MTF represents the loss in resolution due to photocarrier diffusion in the silicon substrate of the uCD prior to collection in specific pixel depletion wells. In the EBS CCD, secondary generation in the silicon from the high energy ele trons can cause additional charge spreading in the silicon. Pixel collection MTF accounts for the uncertainty in position which a photoelectron experiences due to discrete nature of the collecting depletion regions. Transfer MTF represents loss due to finite loss while lens MTF accounts for lens degradation in the imaging system. Tube pretarget MTF accounts for loss in the photocathode/window and electron optics ahead of the CCD.

The noise model for CCD's includes,

- (1) Photon noise (shot noise)
- (2) Fat zero noise
- (3) Dark current noise
- (4) Fast interface state noise (N₃₅)
- (5) Bulk trapping noise (N_T)
- (6) Amplifier noise
- (7) Fixed pattern noise

Expressions for these noise components are fairly well known and will not be discussed here.

Five different types of CCD imagers were analyzed by computer using the display signal-to-noise ratio model described in the preceding sections to predict limiting resolution versus illumination level. More precisely, five different applications of the same CCD array in image sensor configurations were analyzed:

- (1) Direct-view CCD sensor, cooled to T = 210 K, with responsivity of 90 mA/W for 2854 K illumination = 5.6 mA/lm;
- (2) Proximity-focused EBS-CCD tube, operating at T = 300 K, with S-20 extended red response photocathode (responsivity of 7 mA/W for 2854 K illumination = 440 μ A/ ℓ m);
- (3) Proximity-focused EBS-CCD tube, at T = 300 K, with GaAs photo-cathode (responsivity of 6.4 mA/W for 2854 K illumination = 390 μ A/lm);
- (4) EBS-CCD inverter tube, at T = 300 K, with 25 mm S-20 extended red response photocathode;
- (5) CD^{-1} -CCD inverter tube, at T = 300 K, with 25 mm GaAs photocathode.

The CCD array assumed for each of these applications is a thinned, rear-illuminated (or bombarded), 500 x 500-element CCD with a 3:4 aspect ratio, operated in the frame transfer mode with 2:1 interlace (resulting in a possible 500 displayed TV lines). The pixel dimensions are assumed to be 0.9 mil by 1.35 mil, resulting in an active sensor diagonal of 14.3 mm.

Figure 6 and 7 show two representative plots. Figure 6 shows the limiting resolution for a 500 x 500 including system noise and MTF effects for a direct view sensor operating at 210°K with an amplifier dynamic noise of 30 electrons. At this temperature the electron generation is so low for the frame times used that at low light levels amplifier noise dominates. Two types of EBS CCD (gain 2000) are shown for 300°K and a CCD amplifier noise of 150 electrons. For the direct view sensor at low light levels the limiting resolution decreases linearly with irradiance due to amplifier noise limitation. Increasing amplifier noise to 100 electrons will reduce resolution in this range by 3•3.

Relevant parameters used for the calculation are

$$J_D = 10 \text{ nA/cm}^2$$
 at T = 300K
 $N_{SS} = 0$ (Imagers buried channel)
 $T_{eye} = 0.1 \text{ sec.}$
 $T_{FRAME} = 33 \text{ msec}$ (full frame)
Bulk trap density = 0.
Lens cutoff = 150 lp/mm
 $CTE = 10^{-5}$ (500 x 500)
 10^{-4} (160 x 100)

Figure 7 shows calculations for a 160 x 100 imager, with 0.9 mil square pixels, full frame mole (sensor diagonal 4.3mm). All other parameter are the same as for Figure 6 except that the EBS gain is 1000. The Nyquist limit is now 1/2 TVL/PH for the smaller device. Figure 8 shows the effect

of adding fixed pattern noise to the Figure 6 case. A fixed pattern noise of 30 electrons/pixel/frame is added to the direct view sensor and 1000 electrons to the EBS CCD. An example of this type of noise is dark current spikes across the array.

The data presented allow an indication of the performance of EBS CCD's relative to direct view CCD's which shows that the EBS mode is expected to be superior at irradiance levels below about $6 \times 10^{-6} \text{ w/m}^2$. While S20 photocathodes were used in the calculations, results for UV sensitive surfaces can be inferred to be similar from available photocathode QE's.

In summary the calculations show that an EBS CCD offers advantages in low light level applications in the visible which should also apply in the UV. The technology for putting a CCD in a tube has been demonstrated elsewhere. The curves presented represent limiting resolution as determined by observing a display of the CCD image (the $P_{\rm D}$ = ? point). If the image is computer processed prior to image presentation, it may well result in lower values of $P_{\rm D}$ at threshold than indicated here.

APPLICATION TO 400 x 400 CCD IMAGERS

The key problem in using the CCD in a low light level application appears to be in the uniformity of response of the device. Variations for the TI CCD's, as defined by the standard deviation divided by the mean of the pixel response of the total number of pixels in the device can be as low as 8% for broad band 2854°K radiation. The uniformity is generally degraded to some extent at 1900Å, but the best devices show from 10-15% at 4000Å. These uniformity figures generally do not result from isolated blemished pixels but rather from monotonic variations in re-ponse over the active CCD area. It appears that much of the response non-uniformity is

related to non uniformities in the membrane after thinning. These can be non uniform silicon thickness near the edges of the thinning window, surface contamination or spatial variations in the degree of accumulation at the surface. This set of inter-related effects is presently the limiting factor in using CCD imagers at low light levels (both direct view and EBS) and is the focus of a TI internal program to continually increase CCD imager quality. Results of this program will be progressively incorporated into the CCD's made for JPL in the latter part of 1975 and it is expected that these results will significantly improve uniformity of response.

Although the EBS CCD offers the best low light lev_1 performance, the task of putting a large CCD in a tube is by no means a simple one. While this has been demonstrated initially, man, questions remain unanswered concerning the ultimate imaging characteristics of the EBS CCD. For the direct view device, the dynamic noise from the output amplifier ultimately provides the limiting factor at low light levels. Presently the 400 x 400 has an output amplifier consisting of a buried channel reset switch and either BC or SC source follower.

It appears that the dynamic noise, measured on a single pixel using the correlated double sampling technique, is 70-150 electrons. These measurements are taken with a data rate of 1 MHz at 24°C. Measurements at 10 kHz should, however, be performed to allow low frequency characteristics of the MOSFET follower and of the CCD bulk trapping noise and circuitry is presently being assembled to attempt these measurements. The difficulties are related to the 16 sec frame time required to obtain a single sample. About 500 samples will suffice for a representative noise distribution.

It appears that buried channel source follower MOSFETS have lower noise

than surface channel devices. The lowest noise output amplifier appears to be buried channel reset and follower and the noise level (measured on isolated MOSFETS) is about 30 electrons. Changes in dimensions of the source/drain diffusions may allow some reduction in MOSFET noise, but this improvement has not been demonstrated. The measured noise levels of about 100-150 electrons from the CCD probably indicate bulk state trapping noise, although identification requires more data than available at present. Lower amplifier noise will probably require further development.

A program to develop low noise CCD amplifiers is currently in progress at TI. Floating gate amplifier designs are being investigated as well as on chip amplifiers to provide modest gain of 2 - 4X. The results of this program would be available on a continuing basis to impact future JPL designs.

In summary, it is proposed that (a) improvements should be made initially in response uniformity to eliminate spatial fixed pattern noise and (b) that the dynamic noise sources be fully characterized for the 400 x 400 array, preferably at 10 kHz data rates, using the present precharge output amplifier. It is particularly important that such measurements be made, so that development of the total CCD imager can be, at least initially, concentrated in those areas most requiring optimization.

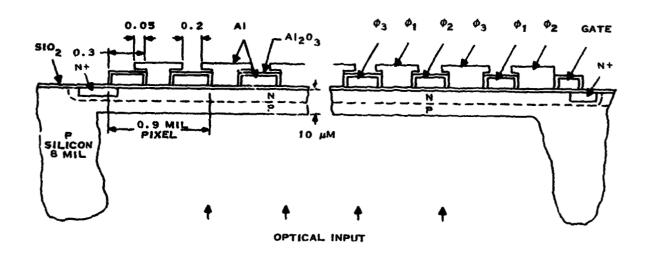


Figure 1. Schematic of thinned, backside illuminated buried channel CCD.

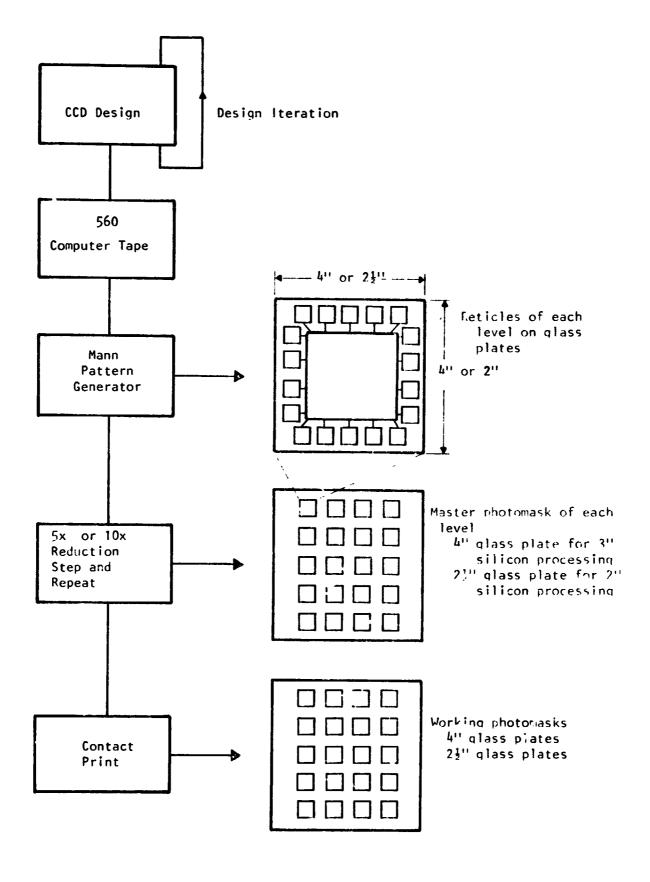


Figure 2. Representation of Photomask Production

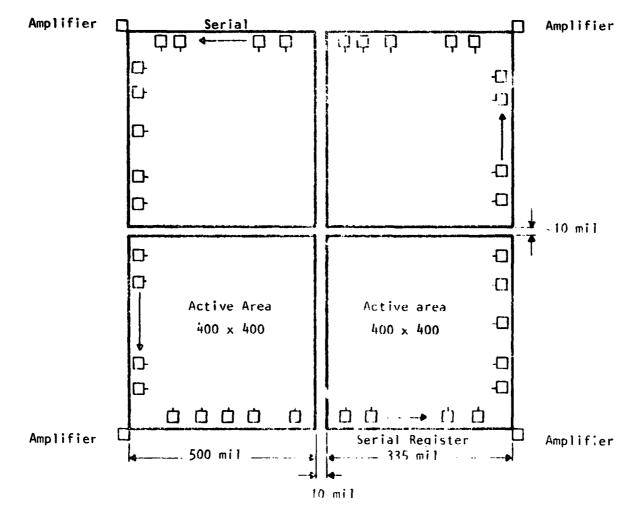


Figure 3. Schematic of four $400 \times 400 \text{ CCO}^4 \text{s}$ in a mosaic.

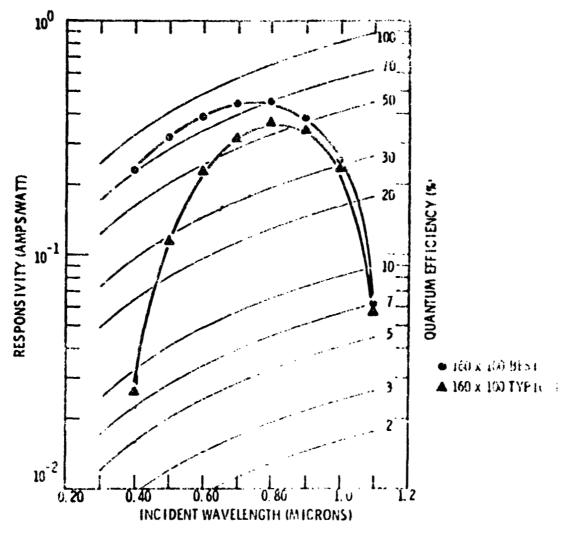


Figure 4. Spectral responsivity of near-ideal and typical thinned backside illuminated CCD area imagers

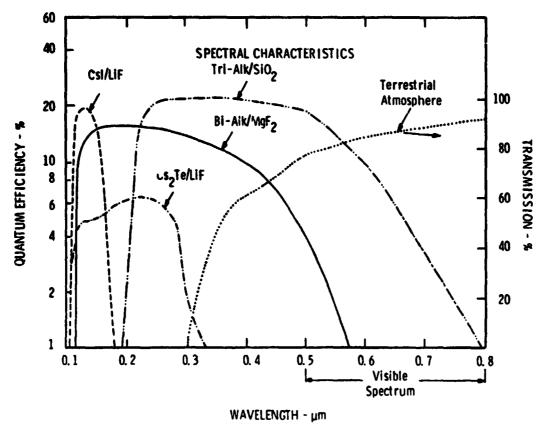
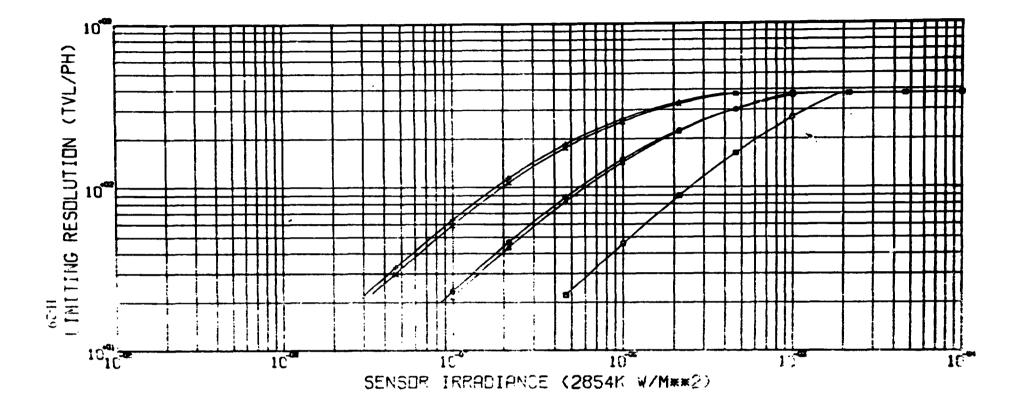


Figure 5. Quantum efficiencies of different photocathode/window combinations as a function of wavelength (Transmission of the earth's atmosphere as a function of wavelength is also presented.)



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Direct-View CCD, T = 210 K, h<sub>ne</sub> = 30 Electrons

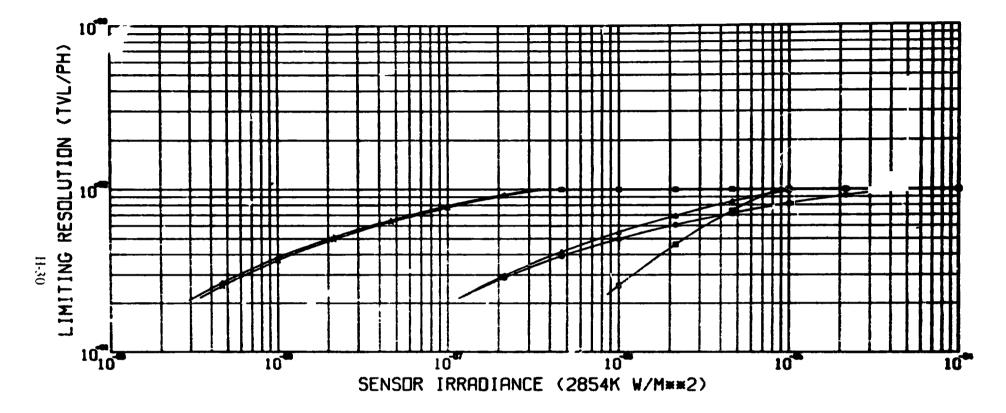
Proximity-Focused EBS-CCD, S-20 Photocathode

Proximity-Focused EBS-CCD, GaAs Photocathode

Inverter EBS-CCD, 25 mm S-20 Photocathode

X Inverter EBS-CCD, 25 mm GaAs Photocathode
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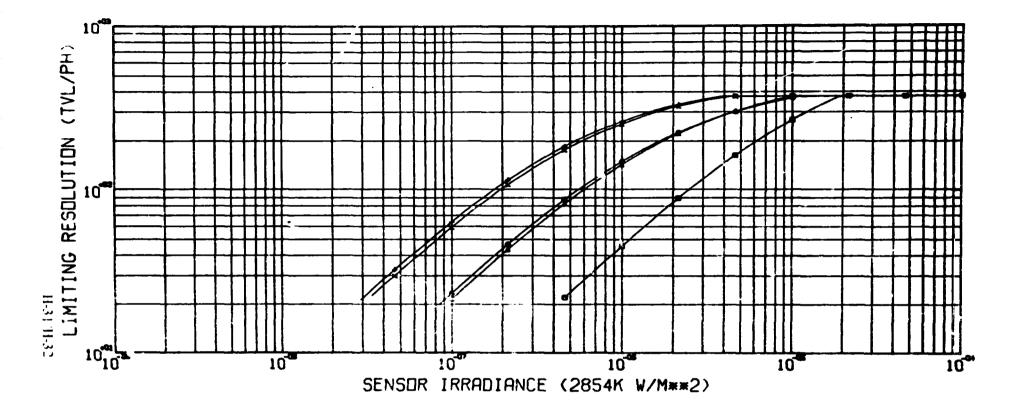
Figure 6. Limiting resolution with System Noise and MTF effect included. Vertical bars in test pattern.



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D Di. sct-View CCD, T = 210 K, h = 30 Electrons
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- O Proximity-Focused EBS-CCD, S-20 Photocathode
- Δ Proximity-Focused EBS-CCD, GaAs Photocathode
- + Inverter EBS-CCD, 25 mm S-20 Photocathode
- X Inverter EBS-CCD, 25 mm GaAs Photocathode

Figure 7. Limiting resolution for 160 \times 100. Full frame, interleaded, 3:1 integration to read out time ratio.



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Direct-View CCD, T = 210 K, N<sub>na</sub> = 30 Electrons
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- O Proximity-Focused EBS-CCD, S-20 Photocathode
- Δ Proximity-Focused EBS-CCD, GaAs Photocathode
- + Inverter EBS-CCD, 25 mm S-20 Photocathode
- X Inverter EBS-CCD, 25 mm GaAs Photocathode

Figure 8. Variation on Figure 6 with fixed pattern noise included.